We provide world-class, leading-edge products and solutions to the world.

TOKYO ELECTRON DEVICE LIMITED has been importing and selling semiconductors since 1965, so we have over 40 years of experience in the market. We have built a strong relationship with Xilinx as a distributor in Japan since 1994, and as Xilinx Alliance Program Member since 2000. We will strengthen cooperation further by supporting Xilinx Targeted Design Platforms strategy and provide our original FPGA platforms, market specific IP Cores and design service in the name of “inrevium”.

Corporate Profile

<table>
<thead>
<tr>
<th>Company Name</th>
<th>TOKYO ELECTRON DEVICE LIMITED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Headquarters</td>
<td>Yokohama East Square 1-4, Kinko-cho, Kanagawa-ku, Yokohama-City, Kanagawa 221-0056</td>
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<tr>
<td>Established</td>
<td>March 3, 1986</td>
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<tr>
<td>Capital</td>
<td>¥2,495,75 million (September 31, 2012)</td>
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<td>Common Stock Listings</td>
<td>The 1st section of the Tokyo Stock Exchange (reg.no.2760)</td>
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<td>Sales</td>
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<td>Group Company</td>
<td>Tokyo Electron Device ASIA PACIFIC LIMITED</td>
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<tr>
<td></td>
<td>Tokyo Electron Device (Shanghai) Limited</td>
</tr>
<tr>
<td></td>
<td>Tokyo Electron Device Singapore Pte. Limited</td>
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<tr>
<td></td>
<td>Shanghai inrevium Solutions Limited</td>
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<tr>
<td></td>
<td>WUXI inrevium Solutions Limited</td>
</tr>
<tr>
<td></td>
<td>PAN ELECTRON Limited</td>
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</table>
Xilinx Alliance Program Premier Member

Tokyo Electron Device is a Premier Member of the Xilinx Alliance Program and delivers the highest level of market- and domain-specific expertise and pre-qualified solutions through Xilinx Targeted Design Platforms. As a Premier Member, TED has gone through a stringent certification process to ensure that its products and services are optimized to streamline customer product development cycles while minimizing risk.

TED supports the Xilinx Targeted Design Platforms strategy and provides original base boards, FMC daughter cards, market-specific, IPs and kits.

Member Levels

<table>
<thead>
<tr>
<th></th>
<th>Premier</th>
<th>Certified</th>
<th>Member</th>
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<td>Lead member for Targeted Design Platforms</td>
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<td>IP optimization for Xilinx (Required)</td>
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<td>Enhanced factory support</td>
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<td>Extensive on-site audit</td>
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<tr>
<td>Qualified via application process</td>
<td>✔️</td>
<td>✔️</td>
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</tbody>
</table>

Xilinx Targeted Design Platform

Focus your time and domain expertise on Differentiation

- Communication – Video – AVB
  - Market specific IP, custom tools, custom boards
- Embedded – DSP – Connectivity
  - Domain IP, Domain tools, FMC daughter cards
- Virtex – Spartan
  - Base IP, ISE program, base boards
Design Service

Opened in 1985, the Design & Development Center uses its wealth of customer project experience and the latest equipment to provide specialized customer design services. The Development Center also creates market specific multi-million gate LSI devices, FPGA evaluation boards, ASIC prototyping boards, drivers, firmware and IP to support a wide range of leading edge applications in the audio, consumer video, broadcast video connectivity, high-speed communication, computer peripheral, medical and industrial automation markets.

Original IP Core

TED develops IP cores for Xilinx FPGAs compliant with new-generation interfaces based on customer needs.
Original Design Manufacturer (ODM)
From the initial stages of determining specifications through to actual manufacture of mass-produced products and implementation of quality control measures, TED provides its customers with a one-stop source to meet their needs. TED aids in the selection, design and development of components scheduled for mass production and strives to optimize costs.

TED is also able to work in collaboration with partner manufacturers in the leading areas of specific fields in order to flexibly respond to customers’ ever-diversifying range of requirements.

Partnership
TED works closely with a number of high-level partners to provide the best FPGA platforms in the market.
Virtex®-7 FPGA ASIC Development Test Platform
Part Number : TB-7V-2000T-LSI

Features
- FPGA
  - XC7V2000T-2FLG1925 device
  - XC7K325T-2FFG900 device
- Memory
  - DDR3 SDRAM (1600Mbps) 2Gbit x 8
- Configuration
  - Supports configuration using MicroSD card or NAND flash memory (Virtex-7 FPGA only)
  - QSPI (Kintex-7 FPGA only)
- Connectors for optional cards
  - High-speed I/O connector (120-pin) x 5
  - FMC HPC (TB-FMCH-VBY1 only)
  - RS-232C (D-sub 9-pin)
- Interfaces
  - DVI (Tx, Rx), UXGA supported
  - USB 2.0/3.0 (device) Type-B
  - PCI Express Gen 2, 8-lane
  - MMCX clock input/output
  - GPIO pin header
- DIP switch, Push switch, LED
- Documentation
  - Hardware User’s Manual
  - Reference Design
  - Schematics
- Power Supply
  * 1) Not all VITA57.1 signals are populated.

Reference Design (Verilog HDL)
- High-speed DDR3 SDRAM Interface Design
  - Memory controller : 1066Mbps, 32bit data width, Generated by Memory Interface Generator (MIG)
- USB 2.0/3.0 Interfaces Design
Zynq™-7000 All Programmable SoC
Extended Microcontroller Board
Part Number: TB-7Z-020-EMC

Features

- FPGA
  - XC7Z020-1CLG484 device
- Memory
  - DDR3 SDRAM 4Gbit x 2 (1GBbyte)
  - Quad SPI Flash 128Mbit
- FMC Interface
  - LPC for FPGA evaluation board (bottom)
  - LPC for FMC IF board (top)
  - FMC Connectors are only exclusive use
- Configuration
  - microSD Card
  - Quad SPI
- Interface
  - DVI TX (micro-HDMI connector)
  - Gigabit Ethernet
  - USB2.0 (Host/Device)
  - SDIO (microSD socket)
  - UART (Pin-header)
  - CAN (Pin-header)
  - JTAG for ARM Processor (Mictor 38)
  - JTAG for FPGA
  - Pmod
- Board size
  - 130mm x 69mm

Reference Design
(Verilog HDL / C code)

- Build In Self Test (BIST)
- AXI Chip2Chip reference design
- IP vendors and debugger vendor provide
  - Reference design for TB-7Z-020-EMC

Block Diagram
Kintex™-7 FPGA ACDC (Acquisition, Contribution, Distribution and Consumption) 1.0 Base Board

Part Number : TB-7K-325T-IMG

Features

▶ FPGA
  – XC7K325T-FFG900 device
▶ Memory
  – DDR3 SDRAM (2Gbit) x 4
▶ FMC Interface*
  – HPC (High Pin Count) x 2
  – LPC (Low Pin Count) x 2
▶ Configuration
  – Via QUAD SPI Flash (128Mbit)
▶ Interfaces
  – MMCX for External Clock
  – JTAG
  – UART (RS-232C D-sub9pin)
  – XADC Pin header
  – DIP Switch, Push button and LED
▶ Board size
  – 240mm x 175mm

* Not all VITA57.1 signals are populated.

Reference Design (Verilog HDL)

▶ HDMI Frame Buffer Design
  – HDMI interface design with TB-FMCH-HDMI2 (sold separately)
  – Memory controller : Generated by Memory Interface Generator (MIG)
▶ EDK Base System Builder Design
  – XDB file for EDK base system builder
  – MicroBlaze™ softcore CPU and peripherals
Kintex-7 FPGA Display Kit
Part Number: TB-7K-ACDC-FND / TB-7K-ACDC-PRO-TV

Features
- TB-7K-325T-IMG Base Board
- FMC Interface
  - HPC (High Pin Count) x 2
  - LPC (Low Pin Count) x 2
- ISE Design Suite
  - PRO: Embedded Edition
  - FND: Logic Edition
  (Device-locked for the Kintex-7 325T FPGA)
- Documentation
  - Hardware Users Manual
  - Reference Design
  - Schematics
- Cables
  - Power Supply
  - Digilent Programming Cable
- Push SW, DIP SW and LED

TB-7K-ACDC-PRO includes
HDMI 2, V-by-One® HS, LVDS
FMC Option Cards

TB-7K-ACDC-FND includes
HDMI 2 FMC Option Card

Reference Design (Verilog HDL)
- Basic Reference design for PRO and FND Kit
  - HDMI Frame Buffer:
    - HDMI Interface (TB-FMCH-HDMI2)
    - Memory controller:
      Memory Interface Generator (MIG) generator
- Reference design for PRO KIT only
  - LVDS reference design
  - V-by-One® HS reference design with time limitation
  - EDK:
    - EDK Base system builder XDB file
    - MicroBlaze soft core CPU
Kintex-7 FPGA Broadcast Video Kit

Part Number : TB-7K-325T-BVK / TB-7K-325T-BVK-RTVE / TB-7K-325T-BVK-VOIP

Features

- Xilinx KC705 Base Board
- Inrevium FMC Card : TB-FMCH-3GSDI2A
  - Input : 2 channel, Output : 2 channel
  - By directional : 2 channel
  - TB-FMCH-3GSDI2A is stackable and can be expanded up to 4ch input, 4ch output and 4ch bidirectional channels by using expansion connector
- ISE Design Suite
  - Embedded Edition (Device-locked for the Kintex-7 325T FPGA)
- Documentation
  - Hardware Users Manual
  - For KC705 via Xilinx web
  - For Option board
  - Reference Design via Xilinx Web
- Cables
  - DIN-BNC (75Ω) Exchange Cable x 3
  - DIN-DIN (75Ω) Cable x 1
  - USB Download Cable (Digilent HS-1)

TB-7K-325T-BVK and TB-7K-325T-BVK-VOIP include
SDI CARD : TB-FMCH-SDI2A

TB-7K-325T-BVK-RTVE includes
SDI CARD : TB-FMCH-SDI2A
HDMI : TB-FMCH-HDMI2

Kintex™-7 FPGA KC705 Feature

- FPGA : XC7K325T-2FFG900C device
- Memory
  - 1GB DDR3 SO-DIMM 1600Mbps
  - 128MB BPI Flash
  - 16MB Quad SPI Flash/8k IIC EPPROM
  - SD Card Slot
- Interface
  - 1000Base-T Ethernet
  - SFP/SFP+ cage
  - GTX port with SMA x 4
  - UART10 USB Bridge
  - PCI Express x 8 edge
  - HDMI Video output
- FMC
  - HPC x 1 (4 GTX, LA and HA)
  - LPC x 1 (1 GTX, LA)
- Clock
  - 200MHz
  - 156.25MHz
- Others
  - Push Buttons
  - DIP Switches
  - LCD

Reference Design (Binary file and Verilog Wrapper)

- Real Time Video Engine
  - Available on Xilinx web site

- SMPTE2022 Video Over IP
  - Available on Xilinx web site
Virtex-7 FPGA PCI Express Gen3 Evaluation Platform

Available: Q2 2013

Part Number: TB-7VX690T-PCIEXP / TB-7VX980T-PCIEXP / TB-7VX1140T-PCIEXP

Features
- Supporting PCI Express Gen3 x 8
- Available 2* DDR3 SDRAM SO-DIMM
- 40ch Rocket IO thorough FMC connector enable total 400Gbps data transfer

Reference Design (Verilog HDL)
- SPCI Express DMA Design with Time limitation
- Memory controller: 1866Mbps (MIG)
- Optical IF loopback design
- Windows7 64bit Driver (Binary)
- Application software (Binary)

Board specification
- FPGA
  - XC7VX690T / XC7VX980T-FFG1926
  - XC7VX1140T-FLG1926
  - FLG1926 and FFG1926 are Pin compatible package
- Memory
  - DDR3 SDRAM SO-DIMM(8 Gbyte) x 2
  - QSPI (128M bit)
- Serdes IF through connector
  - PCI Express (GTH 8 lane)
  - FMC HPC x 4 (GTH 10 lane)
  - SMA (GTH 1 lane)
- Interface
  - FMC HPC x 4
  - MMCX clock input
  - External PLL
  - RS232 (Pin Header)
  - JTAG
  - USB3.0
**Features**

- FPGA
  - Xilinx FPGA: XC6SLX150T-3FFG900 device
- Memory
  - DDR3 SDRAM 1Gbit x 3
- FMC Interface*
  - HPC (high pin count) connector x 1
  - LPC (low pin count) connector x 2
- Configuration
  - SPI Flash 128 Mbit
- Interfaces
  - MMCX clock input
  - USB to PC (via USB-UART conversion device)
  - JTAG
  - DIP Switch, Push button and LED
- Board size
  - 240mm x 175mm

* Not all VITA57.1 signals are populated.

**Reference Design (Verilog HDL)**

- HDMI Frame Buffer Design
  - HDMI interface design with TB-FMCL-HDMI2 (sold separately)
  - Memory controller: 800Mbps, 32bit data width, generated by Memory Interface Generator (MIG).
- EDK Base System Builder Design
  - XDB file for EDK base system builder
  - MicroBlaze™ softcore CPU and peripherals
Spartan-6 FPGA Consumer Video Kit 2.0
Part Number: TB-6S-CVK2-PRO / TB-6S-CVK2-FND

Features
- TB-6S-LX150T-IMG2 base board
- FMC Option Cards (LVDS, V-by-One® HS, DisplayPort, HDMI1.4a)
- ISE® Design Suite: Device-locked for the Spartan-6 LX150T FPGA
- Documentation
  - Getting Start-up Guide
  - Hardware Users Manual
  - Reference Design
  - Schematics
- Cables
  - Power Supply
  - Xilinx Platform Cable USB-II
  - LVDS Cable
  - MMCX to MMCX/SMA Connectors
  - V-by-One HS Cable

TB-6S-CVK2-PRO includes
LVDS, V-by-One® HS, DisplayPort®, and HDMI1.4a FMC Option Cards

TB-6S-CVK2-FND includes
LVDS FMC Option Card

Reference Design (Verilog HDL)
- LVDS Design
  - 7:1 LVDS loop-back test design with TB-FMCL-LVDS
- HDMI1.4 Design
  - Frame split and 2ch output Design, 3D Format data (Side-by-Side)
- V-by-One® HS Design
  - HDMI input to V-by-One HS output Design
  - V-by-One HS loop-back design
- DisplayPort Reference Design
  - DisplayPort interface design
  - (A bitstream data is provided from Xilinx web site for CVK2-PRO)
Large Capacity Extendable PCI Express Gen 2 Platform
Part Number: TB-6V-LX550T, and SX475T-PCIEXP

Features

- **FPGA**
  - Xilinx FPGA: XC6VL550T/ SX475T-2FFG1759 device

- **Memory**
  - DDR3 SDRAM SO-DIMM connector x 2
    - (1Gbyte SO-DIMM modules supplied)
  - SPI Flash 128Mbit

- **PCI Express**
  - Gen 2 x 8 (SX475T supported)
  - Gen 2 x 4 (LX550T supported)

- **FMC Interface**
  - HPC (high pin count) connector x 2
  - LPC (low pin count) connector x 1

- **Configuration**
  - Configuration from micro-SD card
  - High-speed configuration from on-board NAND Flash

- **Interfaces**
  - MMCX clock input
  - External PLL
  - RS-232 (UART)
  - JTAG
  - Pin header
  - DIP Switch, Push button and LED

- **Board size**
  - 300mm x 130mm

Reference Design (Verilog HDL)

- **HDMI Capturing and PCI express DMA Design**
  - HDMI interface design for TB-FMCL-HDMI (sold separately)
  - Memory controller: 800Mbps, 64bit data width,
    Generated by Memory Interface Generator (MIG).
  - DMA design for PCI Express Gen 2 x 8 (except LX550T version)
  - Driver software for Windows 7 / XP, 32bit. (.exe file only)
  - Application software (.exe file only)

* Not all VITA57.1 signals are populated.
<table>
<thead>
<tr>
<th>Platform Part Number</th>
<th>Virtex-7 FPGA</th>
<th>Kintex-7 FPGA</th>
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<td>H-PH</td>
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</tbody>
</table>

※1 Please use the included conversion board.
※2 Direct connection to onboard FMC
◎: Reference design is available.
FPGA Mezzanine Card (FMC) Standard

Developed by a consortium of companies ranging from FPGA vendors to end users, the FPGA Mezzanine Card is an ANSI standard that provides a standard Mezzanine Card form factor, connectors and modular interface to an FPGA located on a base board. Decoupling the I/O interfaces from the FPGA simplifies I/O interface module design while maximizing carrier card reuse.

<table>
<thead>
<tr>
<th>Connector</th>
<th>Pin</th>
<th>User I/O (High Speed Serial I/O)</th>
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<tbody>
<tr>
<td>High Pin Count (HPC)</td>
<td>400pin</td>
<td>168pin (10 channels)</td>
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<tr>
<td>Low Pin Count (LPC)</td>
<td>160pin</td>
<td>72pin (1 channel)</td>
</tr>
</tbody>
</table>

HPC (High Pin Count)

- **3G HD/SD SDI Interface Card**
  - TB-FMCH-3GSDI2A

- **HDMI1.4 Interface Cards**
  - TB-FMCH-HDMI2

- **V-by-One® HS Interface Card**
  - TB-FMCH-VBY1
    - Reference Design
      - V-by-One® HS
      - Tx/Rx Loop Back Design

- **Pin Header Connector Conversion Card**
  - TB-FMCH-PH

- **FMC to FMC Interconnect Cable**
  - TC-FMCH-500

- **Display Port Interface Card**
  - TB-FMCH-DP
    - Standard Ver.1.1a only
    - Reference Design
    - Display Port
    - LogiCORE IP
    - (Bitstream data available from Xilinx website) http://www.xilinx.com/products/ipcenter/EF-DI-DISPLAYPORT.htm
FMC Option Cards

**LPC (Low Pin Count)**

- **Zynq-7000 All Programmable Soc Extension Microcontroller Card**
  - TB-7Z-020-EMC

- **USB3.0 Device Interface Card**
  - TB-FMCL-USB30
    - CYPRESS: CYUSB3014

- **1000 Base-T Ethernet Interface Card**
  - TB-FMCL-GLAN-B

- **24bit/192KHz AD/DA Audio Interface Card**
  - TB-FMCL-ADDA24
    - Input: 2ch  
    - Output: 2ch

- **Pin Header Connector Conversion Cards**
  - TB-FMCL-PH

- **100 Base Ethernet Interface Card**
  - TB-FMCL-INET

- **AES3 Audio Interface Card**
  - TB-FMCL-AUDIO

- **1000 Base-T Ethernet Interface Card**
  - TB-FMCL-GLAN-B

- **LVDS Interface Card**
  - TB-FMCL-LVDS
    - Reference Design
    - LVDS Tx/Rx Loop
    - Back Design (VerilogHDL)
TED provides audio application platform with 3rd party’s network IP for network audio. This solution provides real-time audio transfer via 100 base Ethernet and reduce cables.

**Spartan-6 FPGA Network Audio Platform**

**Audio Platform**
- Low Cost Platform
  - TB-6S-LX25-NAP
- High Performance Platform
  - TB-6S-LX150T-IMG2 (Spartan-6 FPGA)
  - TB-FMCL-GLAN-B (10/100/1000Base Ethernet)
  - TB-FMCL-ADDA24 (Analog Audio IF)

**TB-6S-LX25-NAP Feature**
- 24bit / 192KHz high quality AD/DA converter
- 4ch line input/4ch line output (+4dBu/-10dBV)
- SPDIF digital audio interface In/out
- 100 base Ethernet x 2ch
- Spartan-6 FPGA LX25 Device
- On board VOXO

**TB-FMCL-ADDA24 Feature**
- 24bit / 192KHz high quality AD/DA converter
- 4ch line input/4ch line output (+4dBu/-10dBV)
- On board VOXO
Control interface of factory automation equipment are changed to Ethernet base protocol. These equipment should support new generation, multi-protocol. FPGA solution is very flexible for multi-protocol support and custom requirement.

**Motor Control System**

All required functions (microprocessor, program memory, PWM controller and FA network MAC) of the motor controller can be applied using the FPGA evaluation board "TB-6S-LX25-FNET". FPGA offers the benefits of hardware flexibility.

**Legacy I/F to FA network bridge**

Changing the legacy interface, such as RS-485/RS-232C, to the Ethernet base FA network can be a timely process. The inrevium evaluation platform can be used as a protocol bridge to provide a test environment. FPGA is compatible with various network protocols, thereby eliminating the need to change base.

**Multi network protocol**

It is possible to implement multi-processors with MAC FA network into a single FPGA chip. The FPGA evaluation solution provides hardware flexibility and an interface via FMC option boards to the network gateway, which supports multiple network protocol.
MECHATROLINK-III Master/Slave IP Core

MECHATROLINK-III is highly suited to networks that emphasize precise, synchronous control and high speeds.
MECHATROLINK-III was developed by the MECHATROLINK Members Association as a standard to satisfy the demands of the motion field network market. It boasts higher transmission speeds, faster transmission cycle times and greater transmission distances than ever before, as well as a higher number of maximum slaves.

Features

- Master / Slave Function
- Delivers single chip intelligent function control using FPGA soft-processor with RTOS
- MAX 66MHz Clock, High-speed, Synchronous host interface
- Flexible system configuration by FPGA Logic fabric
  - 16bit/8bit CPU buss, asynchronous buss
  - Zynq AP SoC or Microblaze base SoC

<table>
<thead>
<tr>
<th>Function specifications</th>
<th>MECHATROLINK-III</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical layer</td>
<td>Ethernet</td>
</tr>
<tr>
<td>Transmission cycle time</td>
<td>31.25 µs to 64 ms*</td>
</tr>
<tr>
<td>String size</td>
<td>8/16/32/48/64 bytes (Different string sizes can be used at the same time)</td>
</tr>
<tr>
<td>Number of slaves</td>
<td>62 max</td>
</tr>
<tr>
<td>Maximum transmission distance</td>
<td>100 m between stations 0.5m</td>
</tr>
<tr>
<td>Minimum distance between stations</td>
<td>0.2 m</td>
</tr>
<tr>
<td>Message communications</td>
<td>Available</td>
</tr>
</tbody>
</table>

Core Specifications

- Network: MECHATROLINK-III Network x2 (Port For MII interface 100Mbps Full Duplex mode)
- Host interface: 32bit Joint memory interface / 32bit register interface
- Interrupt: 2 interrupt output
- Bit ordering: little endian
- Deliverable style: Netlist

Target Device

- Spartan-6 FPGA Family

System Configuration Diagram

- Controllers
  - Servo Drivers
  - Inverters
  - Stepping Motor Drivers
  - I/Os
- Servomotors
- Induction motors
- Stepping motors
- Switches, Relays, Valves, Sensors, etc.
The V-by-One®HS standard has been developed by THine Electronics Inc. to offer capabilities for FPD markets that require ever-higher frame rates and resolutions.

Tokyo Electron Device (TED) offers V-by-One®HS IP Core for Xilinx FPGA, reducing costs, time to market and number of cable pairs required.

### Features
- Targets high-speed video signal transmission based on internal connection of equipment.
- Up to 3.75Gbps data rate (effective data rate 3Gbps) per lane.
- Data scrambling and Clock Data Recovery (CDR) to reduce EMI.
- CDR solves the skew problem between clock and data in conventional transfer systems.

### Core Specifications
- Up to 3.75Gbps data rate per lane on Virtex®-6
  (Up to 3.125Gbps on Spartan®-6)
- 1-, 2-, 4- and 8-lane operation
  (Design service for 16 and 32 lanes is available.)
- Variable settings of driver swing, pre-emphasis and equalizer.
- Flexible implementation and package compatibility.

### Target Devices
Core resources of the reference design that has 4-data lanes is shown in the following table. So the smallest devices are available to implement the design including the core.

**Spartan®-6 FPGA Family** : XC6SLX25T (Slices: 30%)
**Virtex®-6 FPGA Family** : XC6VLX75T (Slices: 10%)
Design Service

TED's Design Center boasts a record of over 200 significant development innovations a year. We leverage the design knowledge acquired here to provide our customers with optimized design and development services covering every area from hardware design to the latest technical information from our suppliers, enabling us to engage in even the most complex leading-edge development projects.

Key Technology

High-Speed serial IO
- PCI Express GEN1/GEN2 ×4 to ×16 Lane
- PCI Express GEN3 ×8
- Serial Rapid IO 1G/10G Ethernet

Memory controller
- DDR2 SDRAM-DDR3 SDRAM

Image processing
- CameraLink(Full/Base)  V-by-One HS HDMI DVI

IO
- CameraLink(Full/Base)  V-by-One HS HDMI DVI

Customize

IP Customize Example
- V-by-One HS® IP lane expansion from 8ch to 32ch (8ch x 4)
- Adding image data import design by DDR3 memory controller

Board Customize Example
- Combine two existing boards and create brand new board with two FPGA

Development

Data correcting
- Grabber board: FPGA, Image processing DDR3, SDRAM
- Optical module: SFP/SFP+

Data processing (PC/server)
- Interface board: FPGA, Data transfer DDR3 SDRAM
- Mother board: Processor, LMAX, IO, USB2.0/3.0, SATA

Sensing part
- Camera, Sensor

OEM

Customer requests (Design order) → Development → Preproduction → Production model
- Part selection
- Part procurement

Coordinated to meet customer requests
World Headquarters

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Tokyo Electron Device’s electronic component business has been certified for ISO14001 by Japan Audit and Certification Organization for Environment and Quality (JACO).

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Local
Kintex™-7 FPGA ACDC
(Acquisition, Contribution, Distribution and Consumption) 1.0 Baseboard

The Kintex-7 FPGA ACDC (Acquisition, Contribution, Distribution and Consumption) 1.0 Baseboard. The processing performance and flexibility provided by 28nm Kintex-7 FPGAs allows manufacturers to build stunningly immersive technology into new consumer TV screens that come with features such as multiple windows/picture-in-picture, 3D graphics for games and ultra realistic viewing that goes far beyond HDTV.

- FPGA : Kintex-7 FPGA XC7K325T-FFG900
- Memory : DDR3 2Gbit x 4 (address shared)
- FMC connector
  - HPC (High Pin Count) x 2
  - LPC (Low Pin Count) x 2
- SERDES : 16ch x 12.5Gbps (GTX)