User Manual

TIP-VBY1HS
IP CORE
User Manual

V-by-One® HS Standard IP
for Xilinx FPGA

Rev.1.03

Tokyo Electron Device Ltd.

Revision History

The following table shows the revision history for this document.

Revision	Date	Comments
Rev.1.0.0E	2010/04/12	First Release
Rev.1.0.2E	2012/05/15	Kintex-7 Families Support
Rev.1.0.3E	2015/12/04	Spartan-6 Families and Virtex-6 Families does not support Artix-7 Families, Virtex-7 Families and KintexUltraScale Families Support

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1. Introduction

This chapter introduces the Tokyo Electron Device Ltd.(TED)'s Core that makes up V-by-One® HS standard IP Core "TIP-VBY1HS" designed for Xilinx FPGAs. It also describes design environment for development and provides other related information.

V-by-One® HS standard has been developed by THine Electronics, Inc. to offer capabilities for Flat Panel Display (FPD) markets that are requiring ever-higher frame rates and higher resolutions. This manual provides information about how to edit the TIP-VBY1HS Core's wrapper files and constraint files, and so on.

1.1. About the Core

TIP-VBY1HS Core is a Soft IP designed for Verilog-HDL design environment. It can be implemented in any suitable arrangement with User Logic for the following FPGA families.

・ Hardware Validation

The TIP-VBY1HS Core has acquired a connectivity certification from THine electronics, Inc. by successfully completing a connectivity test between an FPGA board with the IP Core and a V-by-One® HS evaluation board.

・ Target Device

Target devices are the GTP transceivers of Artix-7 families, the GTX transceivers of Kintex-7 families and the GTH transceivers of Virtex-7 families and Kintex UltraScale families.

Note that dependent on FPGA transceiver specifications, the following limitations are imposed on high-speed data lane's transmission bandwidth that is provided by the transceiver.

- **～3.7125Gbps** per data lane (same as the standard)
  - Kintex-7 all speed grade
  - Virtex-7 all speed grade
  - Artix-7 all speed grade
  - Kintex-UltraScale all speed grade

Following equation shows how to determine the data rate of the lane (Gbps).

$$F_{DataRata} = (BIT_{ByteMode} * F_{PixelClk} * 1.25_{(8B/10B)}) / N_{Lane}$$

Example

Byte-mode = 4byte, Pixel Clock frequency = 148.5MHz, Number of data lanes = 2
Data rate per lane = (32bits × 148.5MHz × 1.25) / 2 = **2.97Gbps**

Besides the above, there are other limitations and cautions that are attributed to FPGA specifications and characteristics. For more information, refer to the relevant chapters of this document and the FPGA data sheets.

1.2. Recommended Design Experience

The following development environments are required to develop TIP-VBY1HS Core.

- Synthesis and Implement : Vivado® 2015.3
- Simulation: Mentor Graphics® ModelSim® 10.4b and above

1.3. Additional Core Resources

Besides this document, the following support documentation is available.

- TIP-VBY1HS Data Sheet

1.4. Technical Support

For technical support, go to psd-support@teldevice.co.jp
Tokyo Electron Device Ltd. (TED) provides technical support for this IP Core when used as described in the product documentation. TED cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation.
TED also offers a contract-based development service for customized design or additional function design.

1.5. References

The following V-by-One®HS Standard and FPGA documentations were referenced when developing the TIP-VBY1HS.

- V-by-One®HS Standard Version 1.4 (Dec 15, 2011) by THine Electronics, Inc.
- 7 Series FPGAs GTX/GTH Transceivers (UG476)
- 7 Series FPGAs GTP Transceivers(UG482)
- UltraScale Architecture GTH Transceivers(UG576)
- Kintex-7 FPGA Data Sheet : DC and Switching Characteristics (DS182)
- Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics(DS183)
- Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics(DS181)
- Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics(DS892)

2. Core Architecture

This chapter provides and overview of the TIP-VBY1HS Core architecture.
The TIP-VBY1HS is a full-featured soft IP core that is provided in the form of a NGC Netlist for V-by-One® HS compliant components and a Verilog-RTL for other components.

2.1. Block Diagram

The TIP-VBY1HS Core is partitioned into five major blocks, as shown in Figure 2.1and Figure 2.2.

- **TX_MAIN_LINK.** The signals of this block receive from TX_FORMATTER and send them to the GT_WRAP block.
- **TX_FORMATTER.** This block formats signals from user logic and sends them to the TX_MAIN_LINK block.
- **TX_CLK_RST_GEN.** This block generates all clocks needed for the Transmitter Part.
- **RX_MAIN_LINK.** The signals of this block receive from RX_FORMATTER and send them to the GT_WRAP block.
- **RX_DEFORMATTER.** This block restores formatted data from the RX_MAIN_LINK block and outputs to User Logic.
- **RX_CLK_RST_GEN (Include RX_PLL).** This block generates all clocks needed for the Receiver Part.
- **(GT_WRAP). If you choose parameter “include GT”, this module inside Block Diagram.**

※ If you just only use Transmitter side, you should set the parameter P_TXRX_OFFSEL = 2’b01, and the VX1HS_TOP module will includes TX_MAIN_LINK, TX_FORMATTER, TX_CLK_RST_GEN.

※ If you just only use Receiver side, you should set the parameter P_TXRX_OFFSEL = 2’b10,and the VX1HS_TOP module will includes RXMAIN_LINK, RX_DEFORMATTER, RX_CLK_RST_GEN.

※ If you use both Transmitter and Receiver, you should set the parameter P_TXRX_OFFSEL =2’b11, and the VX1HS_TOP module will includes all modules.

※ If you use GT_WRAP inside VX1HS_TOP, then you should set the parameter P_GT_WRAP_IN=1, else you set the parameter P_GT_WRAP_IN=0.

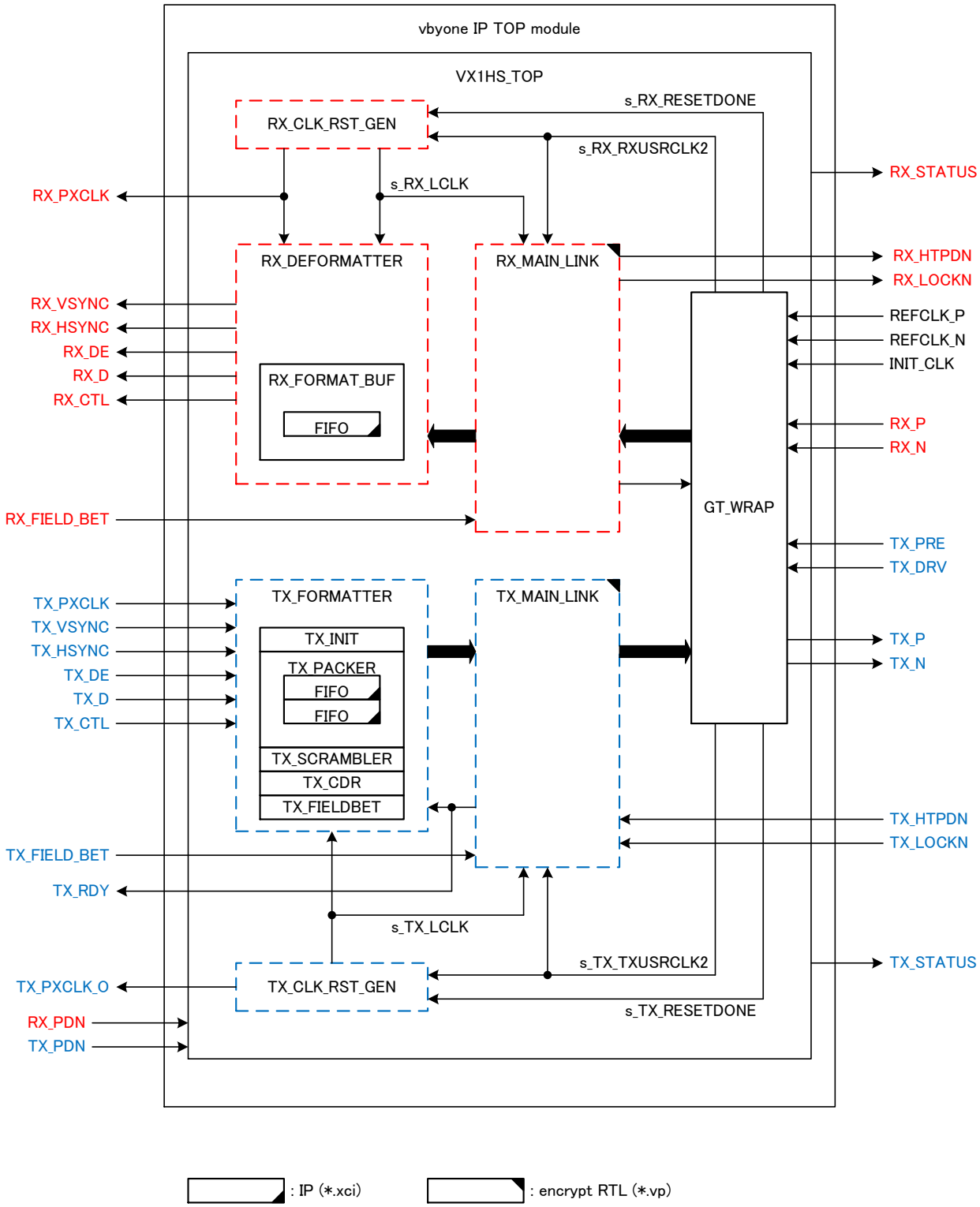

Figure 2.1 Design Top Level Block Diagram (include GT)

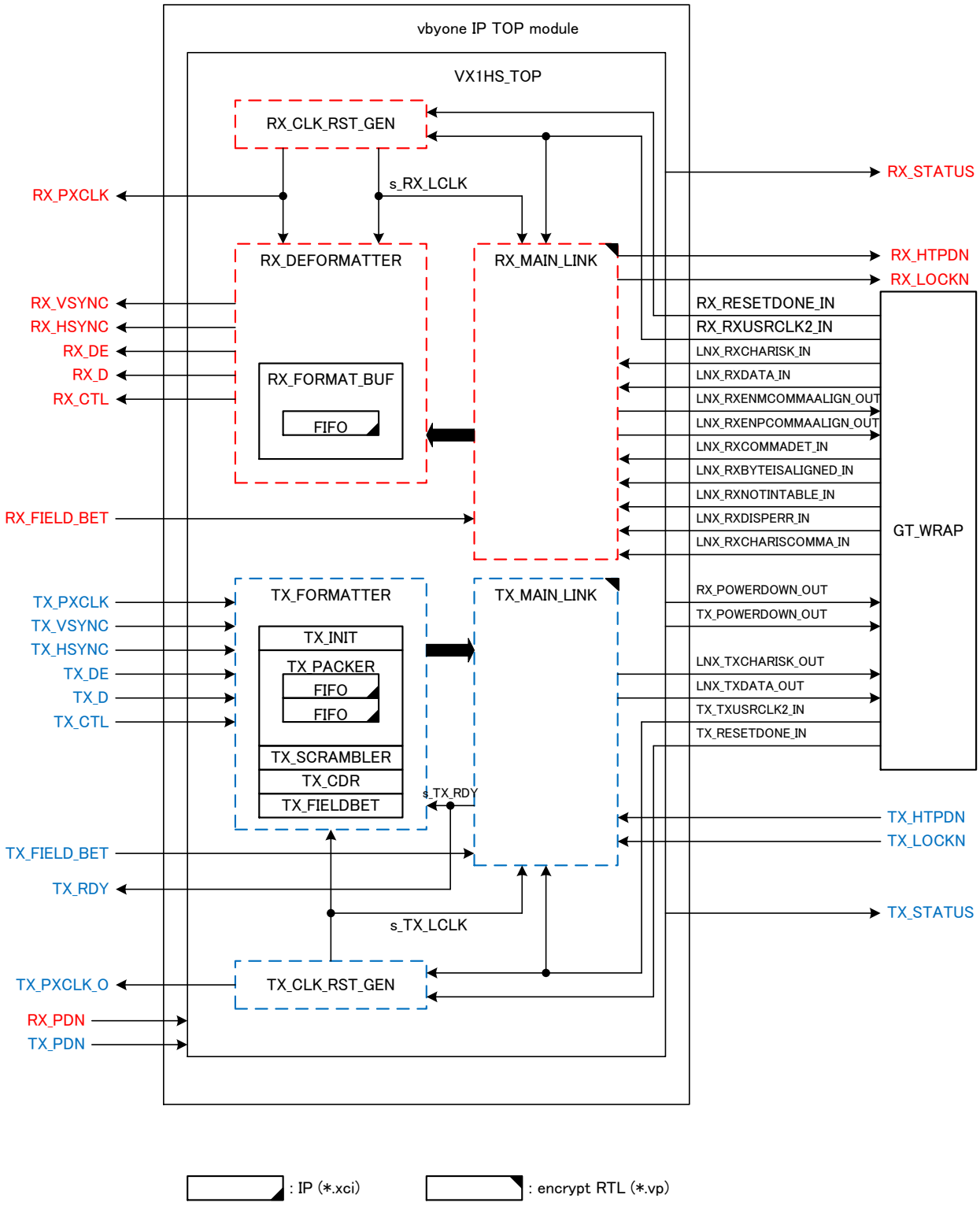

Figure 2.2 Design Top Level Block Diagram (without GT)

2.2. Tranmitter Interfaces

・ General Signals (TX)

Table 2.1 describes the Transmitter General Use signals.

Table 2.1 Transmitter General Use Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_PDN	1	Input	'L'	Power Down

This signal clears and initializes the all functional blocks.

・ Mode Setting Signals (TX)

Table 2.2 describes the Transmitter Mode Setting signals.

Table 2.2 Transmitter Mode Setting Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_FIELD_BET	1	Input	'H'	Field BET Mode Enable

In the mode to check the quality of high-speed serial data lines, the Field BET Mode enables TX_FIELD_BET input to transmitte a data pattern like BET (Bit Error Tester) to the receiver device in Field BET mode and validate it.

・ Video Data Interface (TX)

Table 2.3 describes the Video Data Interface signals of the Transmitter side.

Table 2.3 Transmitter Video Data Interface Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_PXCLK	1	Input	↑	Pixel Clock
TX_VSYNC	P_VNUM	Input	'L'	Vertical sync pulse
TX_HSYNC	P_VNUM	Input	'L'	Horizontal sync pulse
TX_DE	P_VNUM	Input	'H'	Video data enable
TX_DI	40*P_VNUM	Input	-	Video data
TX_CTL	24*P_VNUM	Input	-	Control data (effective in a video blanking period)

(Note) P_VNUM = Lane number / Mapping Lane number

Figure 2.3shows the timing chart of the Video data interface.
Video data is output as effective pixel region when DE is High (active). On the other hand, Control data is output as effective data region when DE is Low (inactive) excluding a period of 1cycle before and after that period.
(Note that there are constraints on this effective period dependent on number of lanes used. For more information, refer to the subsequent description).

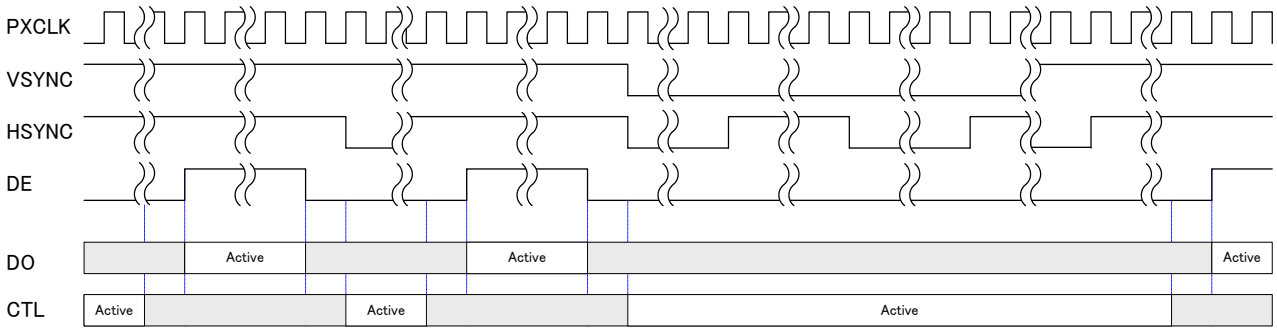

Figure 2.3 Video Data Interface Timing Chart

As shown in Figure 2.4, as the mapping number of data lanes increases, the effective period for Control data is shortened since the ineffective period at both ends increases. This should be considered when using Control data.

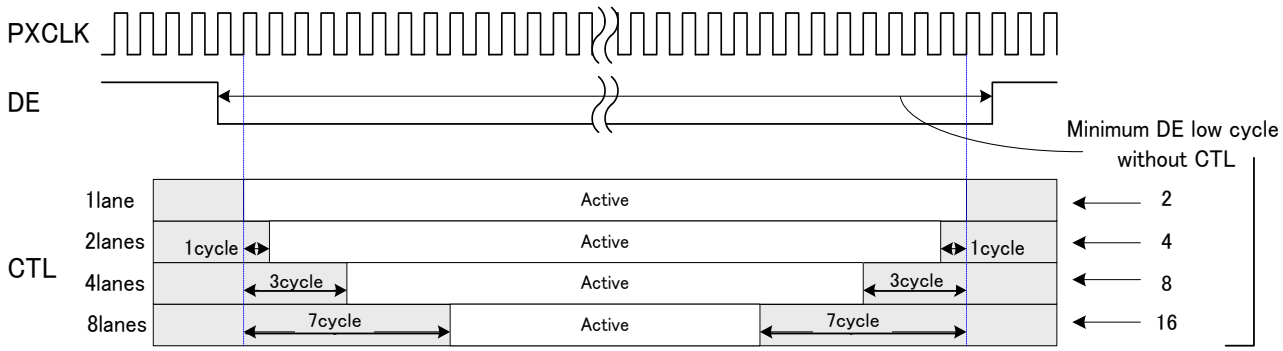

Figure 2.4 Control Data Active Period

・Transceiver and Receiver Interface

・ Table 2.4 describes the Transceiver and Receiver Interface signals of the Transmitter side.

Table 2.4 Transceiver and Receiver Interface Signal of Transmitter Descriptions

Signal Name	Bus width	Direction	Polarity	Description
REFCLK_P	(P_LNUM-1)/8+1	Input	↑	REFCLK of GTX/GTP Transceiver positive
REFCLK_N	(P_LNUM-1)/8+1	Input	↑	REFCLK of GTX/GTP Transceiver negative
INIT_CLK	1	input	↑	free run clock 7series : 74.25MHz Kintex UltraScale: 148.5MHz

(Note)P_LNUM= lane number

・REFCLK_P/N

Two external reference clock input pins are provided for Transceiver and Receiver. They are used to provide a clock to each Tile on the top and bottom sides of FPGA. If only either side of Tile is used, it is not needed to have two clock pins.
For more information about Tile, refer to the Transceivers User Guide.

・Transceiver Interface (TX)

Table 2.5 describes the Transceiver Interface signals of the Transmitter side.

Table 2.5 Transceiver Interface Signal of Transmitter Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_P	P_LNUM	Output	-	High-speed serial Data Lanes positive
TX_N	P_LNUM	Output	-	High-speed serial Data Lanes negative
TX_PXCLK_O	1	Output	↑	Clock output to External PLL
TX_DRV	4	Input	-	Drive Strength Select
TX_PRE	5	Input	-	Pre-Emphasis Select

(Note)P_LNUM= lane number

・TX_P/N

These are external pins of the FPGA for High speed serial video data transmission. Output pins of Transceivers are used.

In the case of using the output pins of Transceiver, the GT_WRAP module shown in Figure 2.1 Block Diagram (section 2.1 “Block Diagram”) is definitely mapped to a Tile.
In the case of 4-Data Lanes, one Tile should be used. In the case of 8-Data Lanes, , two Tiles should be used. In the case of 16-Data Lanes, four Tiles should be used, and in the case of 32-Data Lanes, eight Tiles should be used.

・TX_DRV [3:0], TX_PRE [3:0]

These signal pins are used to set Swing control and Pre-Emphasis control for TX_P/N. They correspond to the following GTH/GTX/GTP port name:

TX_DRV = *txdiffctrl_in, TX_PRE = *txprecursor_in
For characteristics corresponding to these setting values, refer to the associated FPGA

Transceiver User Guide and determine an appropriate value to match the characteristics of device and transmission line to the receiving side.

・ Link Status Signals (TX)

Table 2.6 describes the Link Status signals of the Transmitter side.

Table 2.6 Transmitter Link Status Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_HTPDN	1	Input	'L'	Hot plug detect
TX_LOCKN	1	Input	'L'	Lock detect
TX_RDY	1	Output	'H'	Link Status Ready

・TX_HTPDN

This is an external pin connecting to the equivalent output pin of a receiving end device.
It notifies that the receiveing end device has been connected.

・TX_LOCKN

This is an external pin connecting to the equivalent output pin of a receiving end device.
It notifies that the clock data recovery (CDR) of the receiving end device has been locked.

・TX_RDY

This indicates a Link-up with the receiving end device.
It can be used for a variety of purposes by user logic.

・ for without GT Signals (TX)

Table 2.7 describes the between MGT and MAINLINK signals of the Transmitter side.

Table 2.7 Transmitter Link Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_USERCLK2_IN	1	Input	↑	Clock from MGT
TX_RESET_DONE_IN	1	Input	'H'	Resetdone from MGT
TXPOWERDOWN_OUT	2	Output	'H'	Powerdown to MGT
LNX_TXCHARISK_OUT	2*P_LNUM	Output	-	K character to MGT
LNX_TXDATA_OUT	16*P_LNUM	Output	-	Data to MGT

・TX_USERCLK2_IN

This signal is txuserclk2 that is gtwizard output signal.

・TX_RESET_DONE_IN

This signal is txresetdone that is gtwizard output signal.

・TXPOWERDOWN_OUT

These signals are reset signals. There are used txpd and softreset (reset_tx_pll_and_datapath) of gtwizard.

・LNX_TXCHARISK_OUT

These signals are charisk signals. There are used txcharisk (txctrl2) of gtwizard.

・LNX_TXDATA_OUT

These signals are data signals. There are used txdata of gtwizard.

2.3. Receiver Interfaces

・ General Signals (RX)

Table 2.8 describes the Receiver General Use signals.

Table 2.8 Receiver General Use Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_PDN	1	Input	'L'	Power Down

This signal clears and initializes the all functional blocks.

・ Mode Setting Signals (RX)

Table 2.9 describes the Receiver Mode Setting signals.

Table 2.9 Receiver Mode Setting Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_FIELD_BET	1	Input	'H'	Field BET Mode Enable

In the mode to check the quality of high-speed serial data lines, Field BET Mode enables RX_FIELD_BET input to receive a data pattern like BET (Bit Error Tester)from a transmitting device in Field BET mode and validate it.

・ Video Data Interface (RX)

Table 2.10 describes the Receiver Video Data Interface signals.

Table 2.10 Receiver User Data Interface Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_PXCLK	1	Output	↑	Pixel Clock
RX_VSYNC	P_VNUM	Output	'L'	Vertical sync pulse
RX_HSYNC	P_VNUM	Output	'L'	Horizontal sync pulse
RX_DE	P_VNUM	Output	'H'	Video data enable
RX_DO	40* P_VNUM	Output	-	Video data
RX_CTL	24* P_VNUM	Output	-	Control data (effective in a video blanking period)

(Note) P_VNUM = Lane number / Mapping Lane number

About the timing chart of the Video data interface and the effective period for the Control data, refer to the description of the Transmitter side.

・ Transceiver Interface (RX)

Table 2.11 describes the Transceiver Interface signals of the Receiver side.

Table 2.11 Transceiver Interface Signal of Receiver Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_P	P_LNUM	Input	-	High-speed serial Data Lanes positive
RX_N	P_LNUM	Input	-	High-speed serial Data Lanes negative
RX_RECCLK	1	Output	↑	Recovery Clock output to External PLL

(Note)P_LNUM= lane number

・RX_P/N

These are external pins of the FPGA for High speed serial video data transmission. Input pins of Transceivers are used.

In the case of using the input pins of Transceiver, the GT_WRAP module shown in Figure 2.1 Block Diagram (section 2.1 “Block Diagram”) is definitely mapped to a Tile.
In the case of 4-Data Lanes, one Tile should be used. In the case of 8-Data Lanes, two Tiles should be used. In the case of 16-Data Lanes, four Tiles should be used, and in the case of 32-Data Lanes, eight Tiles should be used.

・ Link Status Signals (RX)

Table 2.12 describes the Receiver Link Status signals.

Table 2.12 Receiver Link Status Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_HTPDN	1	Output	‘L’	Hot plug detect (Selected open drain)
RX_LOCKN	1	Output	‘L’	Lock detect (Selected open drain)
RX_FIELD_BET_ERR	1	Output	‘H’	Filed BET mode Check **Error Status**

・RX_HTPDN

This is an external pin connecting to the equivalent output pin of a transmitting end device.
It notifies the transmitter side of that the receiving end device has been connected.

・RX_LOCKN

This is an external pin connecting to the equivalent output pin of a transmitting end device.
It notifies the transmitter side of that the clock data recovery (CDR) of the receiving end device has been locked.

・RX_FIELD_BET_ERR

This notifies the result of checking in the Field BET mode (“H” in Error).

・ for without GT Signals (TX)

Table 2.7 describes the between MGT and MAINLINK signals of the Transmitter side.

Table 2.13 Transmitter Link Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_USERCLK2_IN	1	Input	↑	Clock from MGT
RX_RESET_DONE_IN	1	Input	'H'	Resetdone from MGT
LNX_RXDATA_IN	16*P_LNUM	input	'H'	Data from MGT
LNX_RXDISPERR_IN	2*P_LNUM	input	-	Disparity error from MGT
LNX_RXNOTINTABLE_IN	2*P_LNUM	input	-	Notintable from MGT
LNX_RXBYTEISALIGNED_IN	P_LNUM	input	-	Byte is aligned from MGT
LNX_RXCOMMADET_IN	P_LNUM	input	-	Comma detect from MGT
LNX_RXCHARISCOMMA_IN	2*P_LNUM	input	-	Comma character from MGT
LNX_RXCHARISK_IN	2*P_LNUM	input	-	K character from MGT
RXPOWERDOWN_OUT	2	output	'H'	Powerdown to MGT
LNX_RXENMCOMMAALIGN_OUT	P_LNUM	output	'H'	Comma minus to MGT
LNX_RXENPCOMMAALIGN_OUT	P_LNUM	output	'H'	Comma plus to MGT

・RX_USERCLK2_IN

This signal is rxuserclk2 that is gtwizard output signal.

・RX_RESET_DONE_IN

This signal is rxresetdone that is gtwizard output signal.

・LNX_RXDATA_IN

These signals are data signals. There are received rxdata of gtwizard.

・LNX_RXDISPERR_IN

These signals are disparity error signals. There are received rxdisperr of gtwizard.

・LNX_RXNOTINTABLE_IN

These signals are notintable signals. There are received rxnotintable of gtwizard.

・LNX_RXBYTEISALIGNED_IN

These signals are byte is aligned signals. There are received rxbyteisaligned of gtwizard.

・LNX_RXCOMMADET_IN

These signals are comma detect signals. There are received rxcommadet of gtwizard.

・LNX_RXCHARISCOMMA_IN

These signals are comma character detect signals. There are received rxchariscomma of gtwizard.

・LNX_RXCHARISK_IN

These signals are K character detect signals. There are received rxcharisk of gtwizard.

・RXPOWERDOWN_OUT

These signals are reset signals. There are used txpd and softreset (reset_tx_pll_and_datapath) of gtwizard.

・LNX_RXENMCOMMAALIGN_OUT

These signals are comma minus signals. There are used rxenmcommaalign of gtwizard.

・**LNX_RXENPCOMMAALIGN_OUT**

These signals are comma plus signals. There are used rxenpcommaalign of gtwizard.

3. Clock Construction

3.1. Tranmitter Clock

Figure 3.1 shows the construction of theTransmitter clock module - **TX_CLK_RST_GEN**.

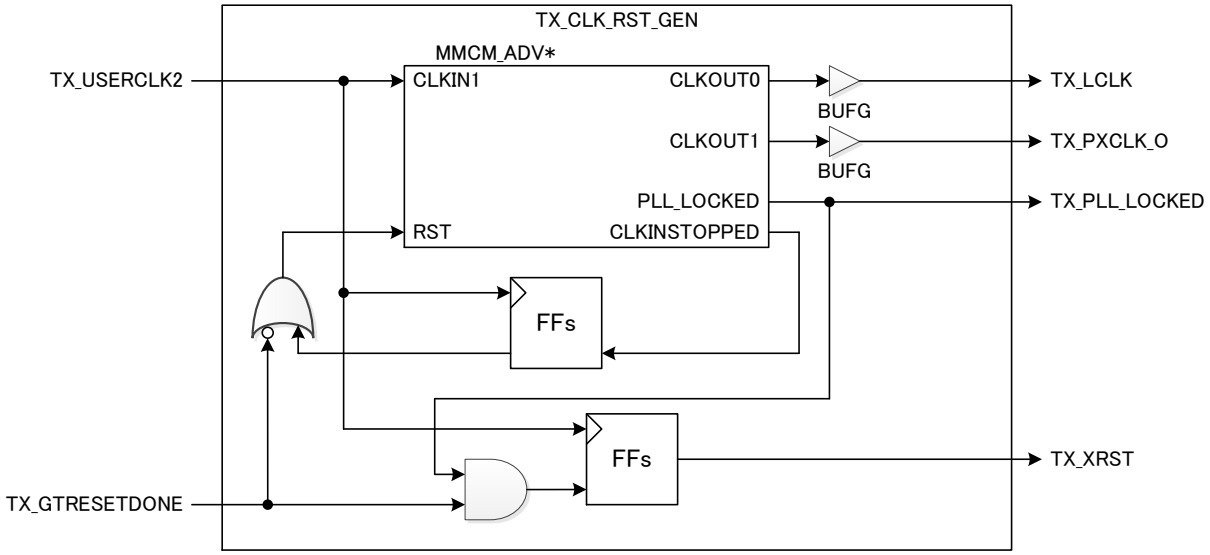

Figure 3.1 TX_CLK_RST_GEN Construction

Table 3.1 describes the TX_CLK_RST_GEN signals.
About the connection of each clock, refer to the Figure 2.1 and Figure 2.2 Top Level Block Diagram.

Table 3.1 TX_CLK_RST_GEN Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
TX_USERCLK2	1	Input	↑	Pixel clock from Video Data Interface
TX_GTRESETDONE	1	Input	'H'	Release of reset from "RESETDONE" port of MGT
TX_PXCLK_O	1	Output	↑	Pixel clock for "TX_FORMATTER" block and user logic
TX_LCLK	1	Output	↑	Clock for adjustment of the signal rate between "TX_FORMATTER" and "FD_MAIN_LINK" block
TX_XRST	1	Output	'L'	System reset for internal logic
TX_PLL_LOCKED	1	Output	'H'	MMCM locked signal

3.2. Receiver Clock

Figure 3.2 shows the construction of the Receiver clock module – **RX_CLK_RST_GEN**.

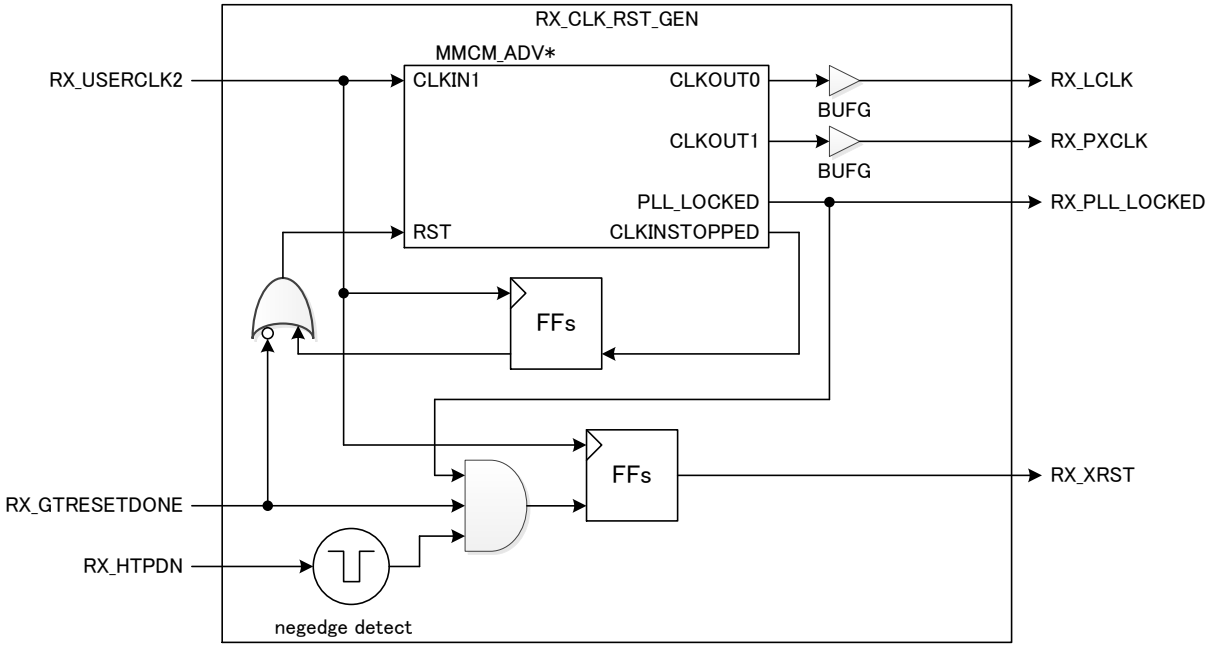

Figure 3.2 RX_CLK_RST_GEN Construction

Table 3.2 describes the RX_CLK_RST_GEN signals.
About the connection of each clock, refer to the Figure 2.1 Top Level Block Diagram.

Table 3.2 RX_CLK_RST_GEN Signal Descriptions

Signal Name	Bus width	Direction	Polarity	Description
RX_USERCLK2	1	Input	↑	Clock input from “GT_WRAP” module
RX_HTPDN	1	input	‘L’	Hot Plug Detect signal from “RX_MAIN_LINK” block
RX_GTRESETDONE	1	input	‘H’	Release of reset from “RESETDONE” port of MGT
RX_PXCLK	1	Output	↑	Pixel clock for Video Data Interface
RX_LCLK	1	Output	↑	Lane clock for adjustment of the signal rate between “RX_MAIN_LINK” and “RX_DEFORMATTER”
RX_PLL_LOCKED	1	Output	‘H’	Locked signal of all PLLs
RX_XRST	1	Output	‘H’	Reset for MGT

4. File Hierarchy Construction

4.1. Folders

Figure 4.1 shows the design folder hierarchy in Transmitter Core.
“RTL” folder contains the all wrapper sources and “ISE” folder contains the all NGC Netlists, constraint files and ISE project of sample design.

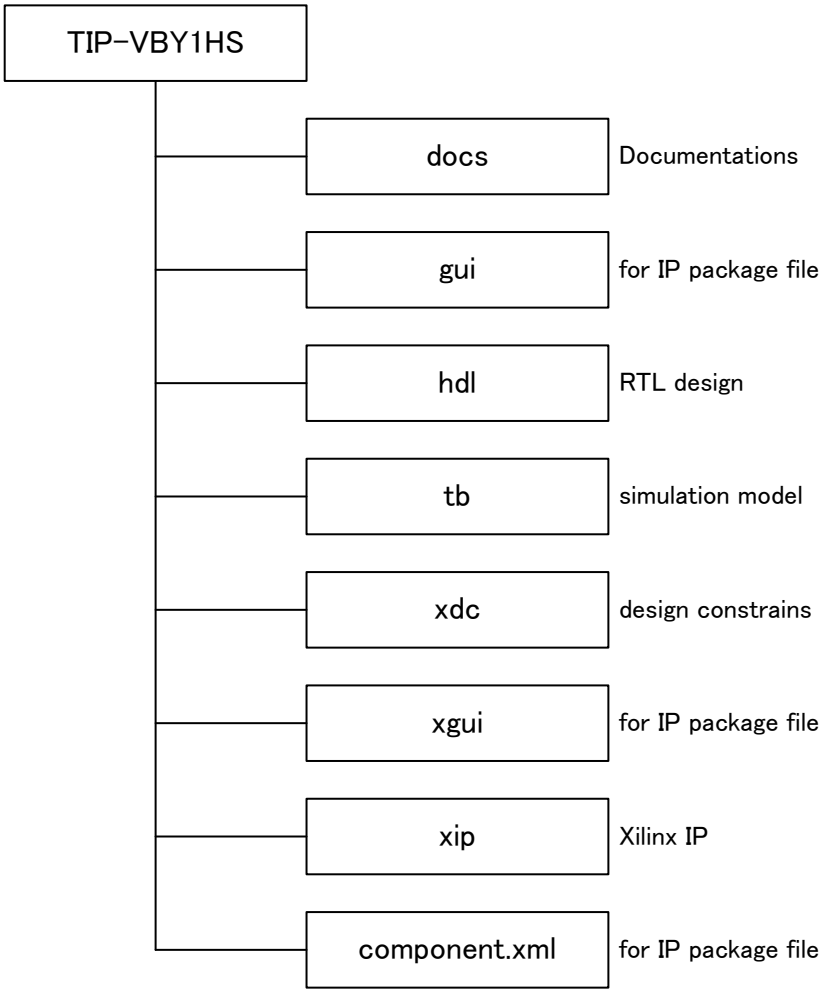

Figure 4.1 TIP-VBY1HS Folder Hierarchy Construction

4.2. Source Files

Figure 4.2 shows the RTL source and Xilinx IP hierarchy.

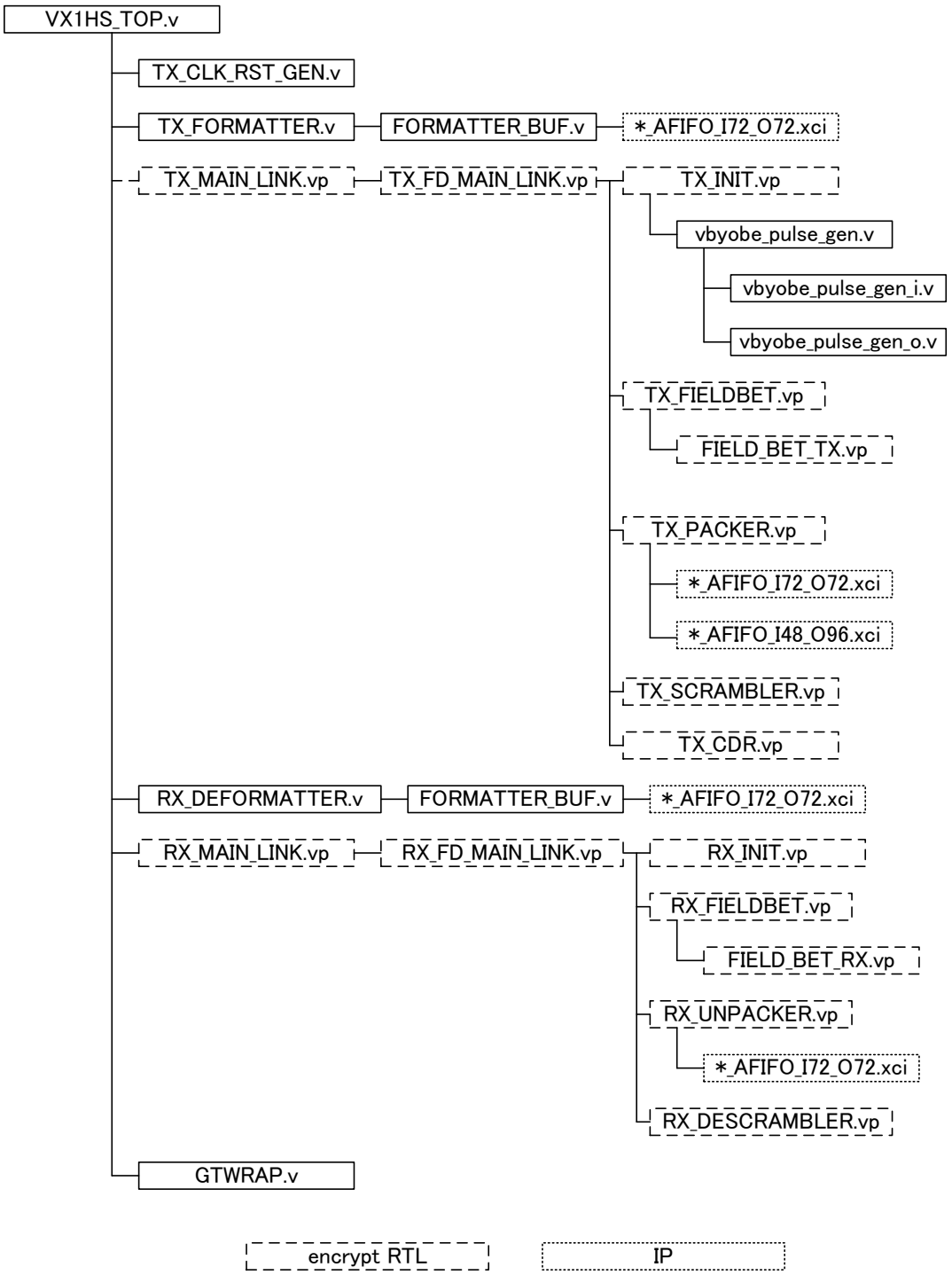

Figure 4.2 VBY1HS Source Hierarchy Construction

5. Parameterization

5.1. Wrapper File

"VX1HS_TOP.v" is a wrapper file that can be regarded as a single hierarchy or used by merging it into the top hierarchy of user logic.

Table 5.1shows the parameters that are defined in the wrapper file **–VX1HS_TOP.v** or the package file.

Table 5.1 Parameterization Table of Wrapper file

Parameter Name	Values	Description
Global		
C_FAMILY	artix7 kintex7 virtes7 kintexu	Target FPGA family
P_GT_WRAP_IN	0, 1	Include GT_WRAP enable 0:disable(without GT_WRAP) 1:enable(include GT_WRAP)
P_BYTE_MD	2'b00 2'b01 2'b10	Byte width of video data and control signal (Byte-mode) 2'b00:3Byte mode 2'b01:4Byte mode 2'b10:5Byte mode 2'b11:reserved
P_TXRX_OFFSEL	2'b01 2'b10 2'b11	Activate Transmitter or Receiver or both 2'b11: Transmitter and Receiver both on 2'b10: only Receiver on 2'b01: only Transmitter on
P_RX_OD	0, 1	Open dorain enable (RX_HTPDN and RX_LOCKN) 0:disable 1:enable
P_LNUM	4, 8, 16, 32	Lane number
P_MNUM	1, 2, 4	Lane Mapping Number (Lane Number / Video Signal)
P_VNUM	P_LNUM / PMNUM	Video Signal Number

parameter C_FAMILY = string , // artix7, kintex7, virtex7 or kintexu

This parameter is used to select a target FPGA type.
Based on this parameter, a dedicated module for Kintex-7 or Virtex-6 or Spartan-6 is called in the merge routine.

parameter P_GT_WRAP_IN = integer , // 1:with GT_WRAP 0:without GT_WRAP

This parameter is selected which include GT_WRAP or without GT_WRAP.

parameter P_TXRX_OFFSEL= interger , // 1:TX on, 2:RX on, 3:RX and TX both on

This parameter is used to activate Transmitter or Receiver or both.

parameter P_BYTE_MD = integer , // Byte Mode 0x0:3byte, 0x1:4byte, 0x2:5byte, 0x3:unused

This parameter is used to set the Byte Mode for Video data interface.
Table 5.2 provides a mapping table between Byte Mode setting and DO/CTL output effective bit width.

Table 5.2 Byte mode Data Mapping

P_BYTE_MD	DO [39:0]	CTL [23:0]
0x0	23:0	7:0
0x1	31:0	15:0
0x2	39:0	23:0

parameter P_RX_OD = integer , // 0:High and Low 1:High-Z and Low

This parameter is used to enable open drain. (for RX_HTPDN and RX_LOCKN)

parameter P_LNUM = integer, // Lane Number

This parameter is Transciever. lane number

parameter P_MNUM = integer , // Lane Mapping Number (Lane Number / Video Signal)

This parameter is Lane Mapping number.
Table 5.3 provides pxclk frequency.

Table 5.3 PXCLK frequency

P_MNUM	TX_PXCLK_O	RX_PXCLK
1	74.25MHz	74.25MHz
2	148.5MHz	148.5MHz
3	297MHz	297MHz

parameter P_VNUM = integer , // Video Signal Number

This parameter is Video signal number.

6. Constraint the Core

A constraint file, vbyone.xdc or vbyone_ooc.xdc, contains timing constraints of major dedicated blocks.

7. Appendix-1

7.1. Byte length and Color mapping

The V-by-One® HS can be used to various types of color video format allocating D[39:0] to pixel data in packer and un-packer mapping. The color data mapping should refer to Table 7.1 and Table 7.2.

Table 7.1 RGB / YCbCr444 / RGBW / RGBY color data mapping

Mode	Packer input & Unpacker output		36bpp RGB /YCbCr444	30bpp RGB /YCbCr444	24bpp RGB /YCbCr444	18bpp RGB /YCbCr444	40bpp RGBW /RGBY	32bpp RGBW /RGBY
5byte mode / 4byte mode / 3byte mode	Byte0	D[0]	R/Cr[4]	R/Cr[2]	R/Cr[0]	-	R[2]	R[0]
		D[1]	R/Cr[5]	R/Cr[3]	R/Cr[1]	-	R[3]	R[1]
		D[2]	R/Cr[6]	R/Cr[4]	R/Cr[2]	R/Cr[0]	R[4]	R[2]
		D[3]	R/Cr[7]	R/Cr[5]	R/Cr[3]	R/Cr[1]	R[5]	R[3]
		D[4]	R/Cr[8]	R/Cr[6]	R/Cr[4]	R/Cr[2]	R[6]	R[4]
		D[5]	R/Cr[9]	R/Cr[7]	R/Cr[5]	R/Cr[3]	R[7]	R[5]
		D[6]	R/Cr[10]	R/Cr[8]	R/Cr[6]	R/Cr[4]	R[8]	R[6]
		D[7]	R/Cr[11]	R/Cr[9]	R/Cr[7]	R/Cr[5]	R[9]	R[7]
	Byte1	D[8]	G/Y[4]	G/Y[2]	G/Y[0]	-	G[2]	G[0]
		D[9]	G/Y[5]	G/Y[3]	G/Y[1]	-	G[3]	G[1]
		D[10]	G/Y[6]	G/Y[4]	G/Y[2]	G/Y[0]	G[4]	G[2]
		D[11]	G/Y[7]	G/Y[5]	G/Y[3]	G/Y[1]	G[5]	G[3]
		D[12]	G/Y[8]	G/Y[6]	G/Y[4]	G/Y[2]	G[6]	G[4]
		D[13]	G/Y[9]	G/Y[7]	G/Y[5]	G/Y[3]	G[7]	G[5]
		D[14]	G/Y[10]	G/Y[8]	G/Y[6]	G/Y[4]	G[8]	G[6]
		D[15]	G/Y[11]	G/Y[9]	G/Y[7]	G/Y[5]	G[9]	G[7]
	Byte2	D[16]	B/Cb[4]	B/Cb[2]	B/Cb[0]	-	B[2]	B[0]
		D[17]	B/Cb[5]	B/Cb[3]	B/Cb[1]	-	B[3]	B[1]
		D[18]	B/Cb[6]	B/Cb[4]	B/Cb[2]	B/Cb[0]	B[4]	B[2]
		D[19]	B/Cb[7]	B/Cb[5]	B/Cb[3]	B/Cb[1]	B[5]	B[3]
		D[20]	B/Cb[8]	B/Cb[6]	B/Cb[4]	B/Cb[2]	B[6]	B[4]
		D[21]	B/Cb[9]	B/Cb[7]	B/Cb[5]	B/Cb[3]	B[7]	B[5]
		D[22]	B/Cb[10]	B/Cb[8]	B/Cb[6]	B/Cb[4]	B[8]	B[6]
		D[23]	B/Cb[11]	B/Cb[9]	B/Cb[7]	B/Cb[5]	B[9]	B[7]
	Byte3	D[24]	-	-	-	-	R[0]	-
		D[25]	-	-	-	-	R[1]	-
		D[26]	B/Cb[2]	B/Cb[0]	-	-	G[0]	-
		D[27]	B/Cb[3]	B/Cb[1]	-	-	G[1]	-
		D[28]	G/Y[2]	G/Y[0]	-	-	B[0]	-
		D[29]	G/Y[3]	G/Y[1]	-	-	B[1]	-
		D[30]	R/Cr[2]	R/Cr[0]	-	-	W/Y[0]	-
		D[31]	R/Cr[3]	R/Cr[1]	-	-	W/Y[1]	-
	Byte4	D[32]	-	-	-	-	W/Y[2]	W/Y[0]
		D[33]	-	-	-	-	W/Y[3]	W/Y[1]
		D[34]	B/Cb[0]	-	-	-	W/Y[4]	W/Y[2]
		D[35]	B/Cb[1]	-	-	-	W/Y[5]	W/Y[3]
		D[36]	G/Y[0]	-	-	-	W/Y[6]	W/Y[4]
		D[37]	G/Y[1]	-	-	-	W/Y[7]	W/Y[5]
		D[38]	R/Cr[0]	-	-	-	W/Y[8]	W/Y[6]
		D[39]	R/Cr[1]	-	-	-	W/Y[9]	W/Y[7]

Table 7.2 YCbCr422 color data mapping

Mode			Packer input & Unpacker output		32bpp /YCbCr422	24bpp /YCbCr422	20bpp /YCbCr422	16bpp /YCbCr422
5byte mode	4byte mode	3byte mode	Byte0	D[0]	Cb/Cr[8]	Cb/Cr[4]	Cb/Cr[2]	Cb/Cr[0]
				D[1]	Cb/Cr[9]	Cb/Cr[5]	Cb/Cr[3]	Cb/Cr[1]
				D[2]	Cb/Cr[10]	Cb/Cr[6]	Cb/Cr[4]	Cb/Cr[2]
				D[3]	Cb/Cr[11]	Cb/Cr[7]	Cb/Cr[5]	Cb/Cr[3]
				D[4]	Cb/Cr[12]	Cb/Cr[8]	Cb/Cr[6]	Cb/Cr[4]
				D[5]	Cb/Cr[13]	Cb/Cr[9]	Cb/Cr[7]	Cb/Cr[5]
				D[6]	Cb/Cr[14]	Cb/Cr[10]	Cb/Cr[8]	Cb/Cr[6]
				D[7]	Cb/Cr[15]	Cb/Cr[11]	Cb/Cr[9]	Cb/Cr[7]
			Byte1	D[8]	Y[8]	Y[4]	Y[2]	Y[0]
				D[9]	Y[9]	Y[5]	Y[3]	Y[1]
				D[10]	Y[10]	Y[6]	Y[4]	Y[2]
				D[11]	Y[11]	Y[7]	Y[5]	Y[3]
				D[12]	Y[12]	Y[8]	Y[6]	Y[4]
				D[13]	Y[13]	Y[9]	Y[7]	Y[5]
				D[14]	Y[14]	Y[10]	Y[8]	Y[6]
				D[15]	Y[15]	Y[11]	Y[9]	Y[7]
			Byte2	D[16]	-	-	-	-
				D[17]	-	-	-	-
				D[18]	-	-	-	-
				D[19]	-	-	-	-
				D[20]	-	-	-	-
				D[21]	-	-	-	-
				D[22]	-	-	-	-
				D[23]	-	-	-	-
			Byte3	D[24]	Y[2]	-	-	-
				D[25]	Y[3]	-	-	-
				D[26]	Cb/Cr[2]	-	-	-
				D[27]	Cb/Cr[3]	-	-	-
				D[28]	Y[6]	Y[2]	Y[0]	-
				D[29]	Y[7]	Y[3]	Y[1]	-
				D[30]	Cb/Cr[6]	Cb/Cr[2]	Cb/Cr[0]	-
				D[31]	Cb/Cr[7]	Cb/Cr[3]	Cb/Cr[1]	-
			Byte4	D[32]	Y[0]	-	-	-
				D[33]	Y[1]	-	-	-
				D[34]	Cb/Cr[0]	-	-	-
				D[35]	Cb/Cr[1]	-	-	-
				D[36]	Y[4]	Y[0]	-	-
				D[37]	Y[5]	Y[1]	-	-
				D[38]	Cb/Cr[4]	Cb/Cr[0]	-	-
				D[39]	Cb/Cr[5]	Cb/Cr[1]	-	-

7.2. Allocation of pixel to Data Lane

Depend on the data rate and pixel color depth, it is permitted to increase the Data Lanes. About the multiple Data Lanes combination, Refers to Figure 7.1.

The V-by-One® HS compliant components must be implemented with at least one Data Lane. If the data rate of the required color depth and timing is higher than the components maximum supported data rate, additional Data Lane can be used. (The maximum data rate of V-by-One® HS Data Lane is 3.75Gbps per lane.) In this case, total lane count should be even number, under the condition of the fewer lane number.
The pixel number for the horizontal active and blanking term (H-active, H-blank) should be adjusted to become the multiple number of the lane count.

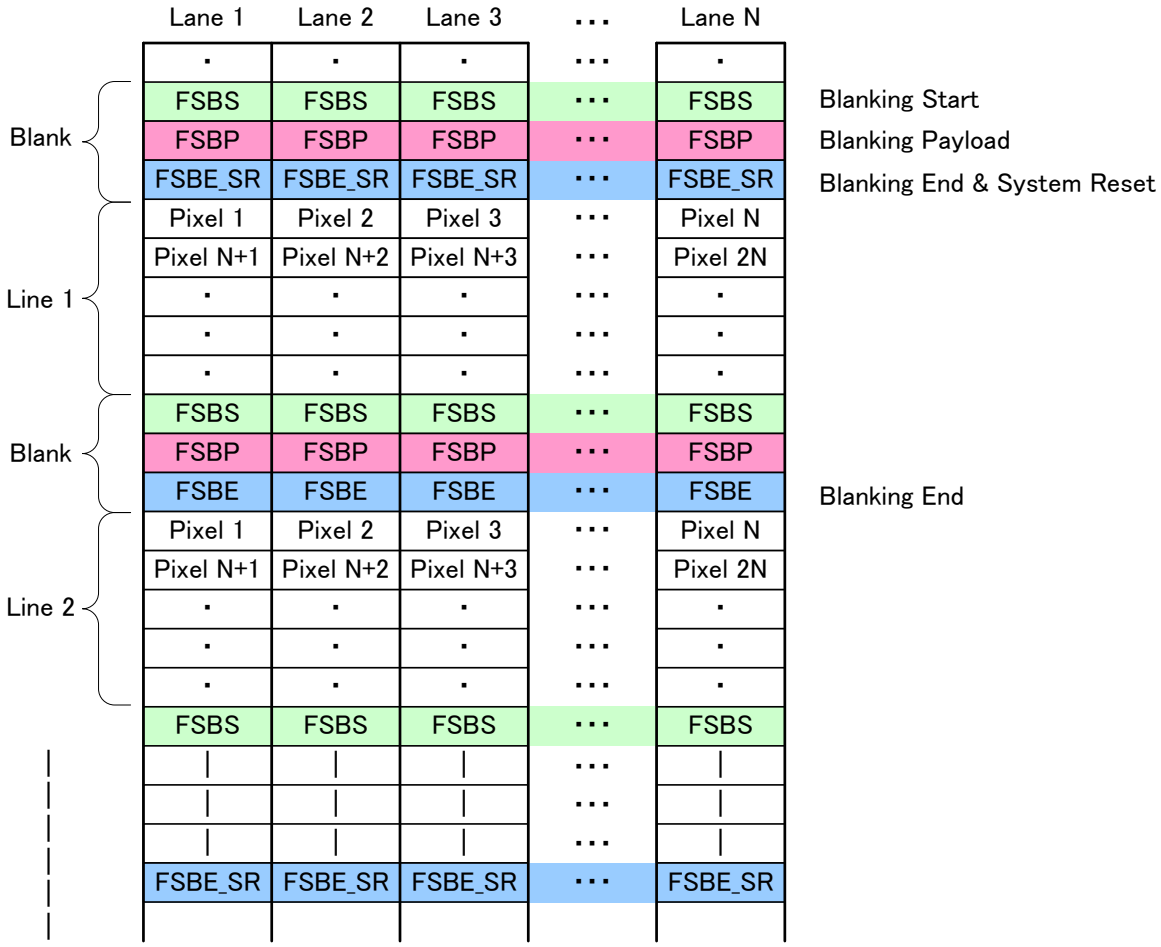

Figure 7.1 Allocation of pixel to Data Lane

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