TB-7K-325T-IMG
FMC Connector Pin Assign

Rev.1.01

Revision History

Version	Date	Description	Publisher
Rev.1.00	2012/05/11	Preliminary version	Yoshioka
Rev.1.01	2012/05/29	Modified LPC1 and LPC2: non differential signal pin	Yoshioka

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1. Related Documents and Accessories

Related documents:

Please refer to following documentations of TB-7K-325-IMG.

- Hardware User Manual
- Schematic
- Reference design and related documentations

Latest documentation is available at TED Support Web.

2. Overview

This document describes the pin-assign of FPGA Mezzanine Card(FMC) connectors on TB-7K-325T-IMG FPGA evaluation board. FMC is ANSI/VITA57 Standard.

TB-7K-325T-IMG has two High-Pin Count(HPC) connectors and two Low-Pin Count(LPC) connectors. **All pin of each FMC connectors are not connected to FPGA.** Please see related documentations and confirm that signals connections before using.

3. Connected Signals

3.1. HPC1

3.1.1. Connected Signals

GBTCLK0_M2C_P/N : Connected to FPGA directly.

GBTCLK1_M2C_P/N : Via clock selector chip.

DP_M2C_P/N[7:0], DP_C2M_P/N[7:0]

CLK0_M2C_P/N, CLK1_M2C_P/N, CLK2_M2C_P/N, CLK3_M2C_P/N

LA_P/N[33:0]

HA_P/N[00], HA_P/N[01], HA_P/N[02], HA_P/N[04], HA_P/N[05], HA_P/N[06], HA_P/N[08], HA_P/N[09], HA_P/N[10], HA_P/N[12], HA_P/N[13], HA_P/N[17]

HB_P/N[00], HB_P/N[02], HB_P/N[03], HB_P/N[04], HB_P/N[05], HB_P/N[06], HB_P/N[08], HB_P/N[09], HB_P/N[10], HB_P/N[12], HB_P/N[13], HB_P/N[14]

3.1.2. Non deferential IO

HA_P/N[05], HA_P/N[13], HB_P/N[04], HB_P/N[05]

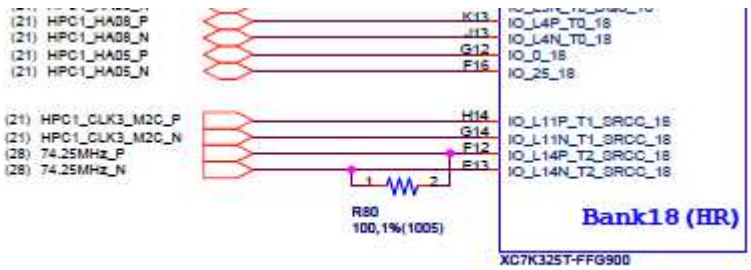

Figure 3-1 Non differential IO (HPC1)

3.2. HPC2

3.2.1. Connected Signals

GBTCLK0_M2C_P/N : Connected to FPGA directly.
GBTCLK1_M2C_P/N : Via clock selector chip.
DP_M2C_P/N[7:0], DP_C2M_P/N[7:0]

CLK0_M2C_P/N, CLK1_M2C_P/N

LA_P/N[33:0]

3.3. LPC1

This section describes LPC connection.

3.3.1. Connected Signals

CLK0_M2C_P/N, CLK1_M2C_P/N

LA_P/N[33:0]

3.3.2. Non deferential IO

LA_P/N[12], LA_P/N[22]

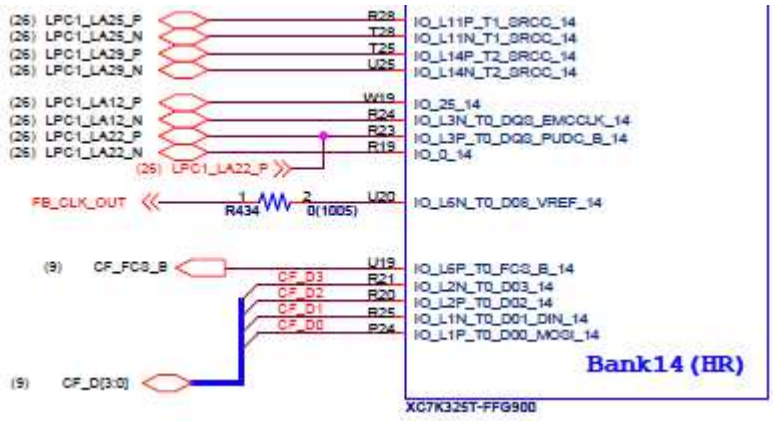

Figure 3-2 Non deferential IO (LPC1)

3.4. LPC2

This section describes LPC connection.

3.4.1. Connected Signals

CLK0_M2C_P/N, CLK1_M2C_P/N

LA_P/N[33:0]

3.4.2. Non deferential IO

LA_P/N[25], LA_P/N[29]

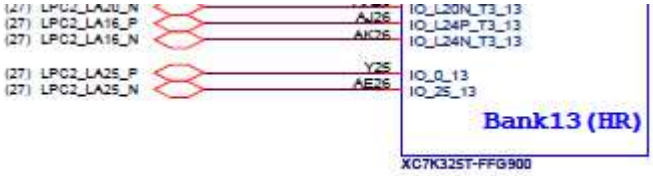

Figure 3-3 Non differential IO (LPC2)

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