

TB-FMCH-VBY1-AD

Hardware User Manual

Rev.1.00

Revision History

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Table of Contents

| | |
|---|----|
| 1. Related Documents and Accessories | 8 |
| 2. Overview | 8 |
| 3. Feature | 9 |
| 4. Block Diagram | 10 |
| 5. External View of the Board | 11 |
| 6. Board Specifications | 12 |
| 7. Description of Components | 13 |
| 7.1. Signal connections between SerDes/LVDS and FMC connectors..... | 13 |
| 7.2. Customization of the SerDes connector..... | 18 |
| 7.3. Power supply to the connector..... | 20 |
| 7.4. Option pin configuration of the VBY1-RX (J2) connector..... | 20 |
| 7.5. Option pin configuration of the VBY1-TX (J3) connector | 21 |
| 7.6. Option pin configuration of connectors..... | 21 |
| 7.7. Reference Clock..... | 22 |
| 7.7.1. Output frequency setting..... | 23 |
| 7.7.2. Changing I2C setting | 23 |
| 7.7.3. FMC to PLL Connection | 24 |
| 7.7.4. PLL STATUS Output..... | 24 |
| 8. Default Switch Settings | 25 |

List of Figures

| | |
|--|----|
| Figure 3-1 FMC Connector Pin Layout | 9 |
| Figure 4-1 Block Diagram | 10 |
| Figure 5-1 Component Side | 11 |
| Figure 5-2 Solder Side | 11 |
| Figure 6-1 Board Dimensions | 12 |
| Figure 7-1 Supplied Cables..... | 13 |
| Figure 7-2 Cable Connections | 13 |
| Figure 7-3 An example of the V-by-one HS 16LANE structure..... | 18 |
| Figure 7-4 Overview image of the FI-RE41S-VF board..... | 18 |
| Figure 7-5 SerDes/LVDS CN Power Supply | 20 |
| Figure 7-6 A Tri-State Buffer Structure | 20 |
| Figure 7-7 VBY1-TX(J3) Option Pin Connections..... | 21 |
| Figure 7-8 LVDS-1(CN1) Test Points | 21 |
| Figure 7-9 LVDS-1(CN2) Test Points | 21 |
| Figure 7-10 VBY1-TX(J3) Test Points | 22 |
| Figure 7-11 PLL Connection Diagram..... | 22 |
| Figure 7-12 PLL I2C Connection Diagram | 23 |

List of Tables

| | |
|--|----|
| Table 7-1 VBY1-RX (J2) Signal Connection | 14 |
| Table 7-2 VBY1-TX (J3) Signal Connection | 15 |
| Table 7-3 LVDS-1 (CN1) Signal Connection | 16 |
| Table 7-4 LVDS-2 (CN2) Signal Connection | 17 |
| Table 7-5 VBY1-RX(J2) with FI-RE41S-VF Signal Connection | 19 |
| Table 7-6 VBY1-TX(J3) with FI-RE41S-VF Signal Connection..... | 19 |
| Table 7-7 Power Supply Switching..... | 20 |
| Table 7-8: FMC to PLL Signal Connection | 24 |
| Table 7-9 PLL LED STATUS..... | 24 |
| Table8-1 Default Settings | 25 |

Introduction

Thank you for purchasing the **TB-FMCH-VBY1-AD** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual and then always keep it handy.




SAFETY PRECAUTIONS

Be sure to observe these precautions




Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- Before using the product, read these safety precautions carefully to assure correct use.
- These precautions contain serious safety instructions that must be observed.
- After reading through this manual, be sure to always keep it handy.

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

| | |
|--|--|
|  Danger | Indicates the high possibility of serious injury or death if the product is handled incorrectly. |
|  Warning | Indicates the possibility of serious injury or death if the product is handled incorrectly. |
|  Caution | Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly. |

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

| | |
|---|---------------------------------|
|  | Turn off the power switch. |
|  | Do not disassemble the product. |
|  | Do not attempt this. |



Warning

| | |
|--|---|
| | <p>In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.</p> |
| | <p>If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.</p> |
| | <p>Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.</p> |
| | <p>Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.</p> |
| | <p>Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.</p> |
| | <p>If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.</p> |
| | <p>Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.</p> |
| | <p>Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.</p> |
| | <p>Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.</p> |
| | <p>Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.</p> |

**Caution****Do not use or place the product in the following locations.**

- Humid and dusty locations
- Airless locations such as closet or bookshelf
- Locations which receive oily smoke or steam
- Locations exposed to direct sunlight
- Locations close to heating equipment
- Closed inside of a car where the temperature becomes high
- Sticky locations
- Locations close to water or chemicals

Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.

**Do not place heavy things on the product.**

Otherwise, the product may be damaged.

Disclaimer

This product is a Samtec FMC connector to JAE FI-R Series connector conversion board. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- (1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- (2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
- (3) Use of this product against the instructions given in this manual.
- (4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

- (1) Erasure or corruption of data arising from use of this product.
- (2) Any consequences or other abnormalities arising from use of this product, or
- (3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Board Accessories:

Dedicated cables

- V-by-One HS x 2, LVDS x 1

FMC Spacer set

- Spacer x 2, Screws x 4

Jumper short-circuit socket

- Short-circuit socket x 10

2. Overview

This product is a Samtec FMC connector (High-Pin Count) to JAE FI-R Series connector conversion board. It supports Thine Electronics' V-by-One HS high speed data interface.

For 16 lane configuration, it is required 41 pin connector (FI-RE41S-VF). Please refer to section 7.2 and contact to us.

The Board is specifically designed for connection with a platform board equipped with High-Pin Count connectors.

3. Feature

- FMC Connector: Samtec FMC Connector (High-Pin Count)
- SerDes/LVDS Connector: JAE FI-R Series Connector
- Clock Supply: Clock can be supplied from IDT ICS849N2021 to Xilinx FPGA transceiver
- Power Supply Switchover: Power supply switchover is enabled by an onboard jumper switch

| | K | J | H | G | F | E | D | C | B | A |
|----|------------|------------|-------------|------------|-----------|-----------|---------------|-----------|---------------|-----------|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | RES1 | GND |
| 2 | GND | CLK3_M2C_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_M2C_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_M2C_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_M2C_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | GND | DP7_M2C_N | GND |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP8_M2C_P | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_N | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

Figure 3-1 FMC Connector Pin Layout

4. Block Diagram

Figure 4-1 shows a block diagram of the TB-FMCH-VBY1-AD board. The FMC connector is mounted on the reverse side of the board.

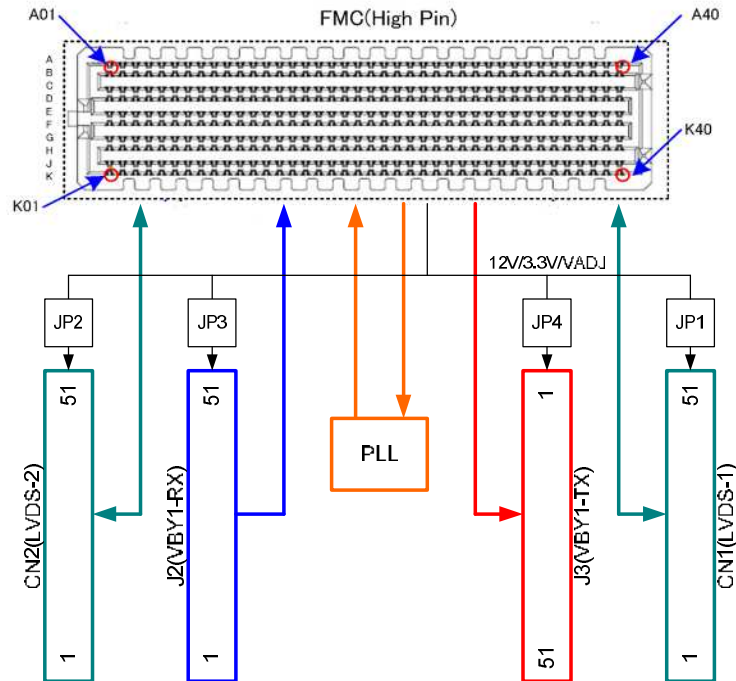


Figure 4-1 Block Diagram

Major functions:

- 8 pairs SerDes connection for each FMC connector to SerDes connector (J2/J3) circuit
- 12 pairs LVDS connection for each FMC connector to LVDS connector (CN1/CN2) circuit
- Power supply to the SerDes/LVDS connector
- Reference clock to Xilinx FPGA transceiver
- Probe points

5. External View of the Board

Figures 5-1 and 5-2 show the external view of the board.

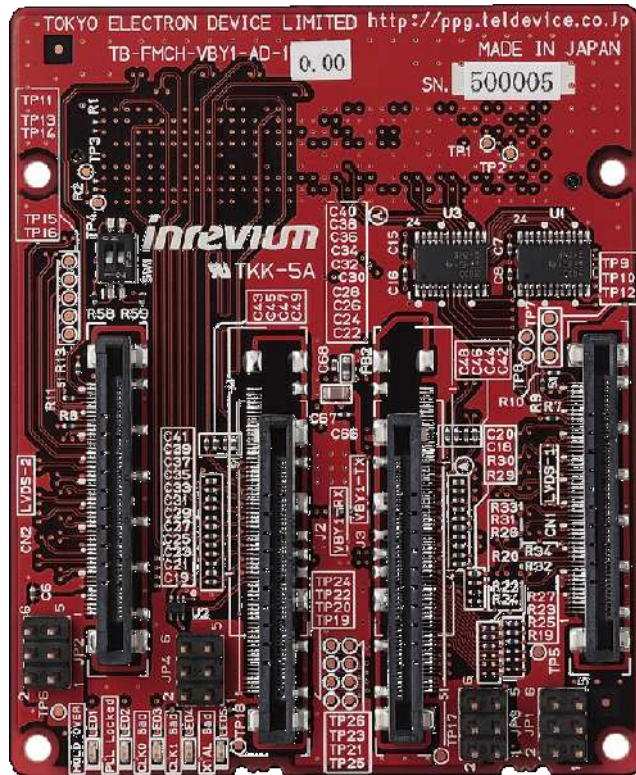


Figure 5-1 Component Side

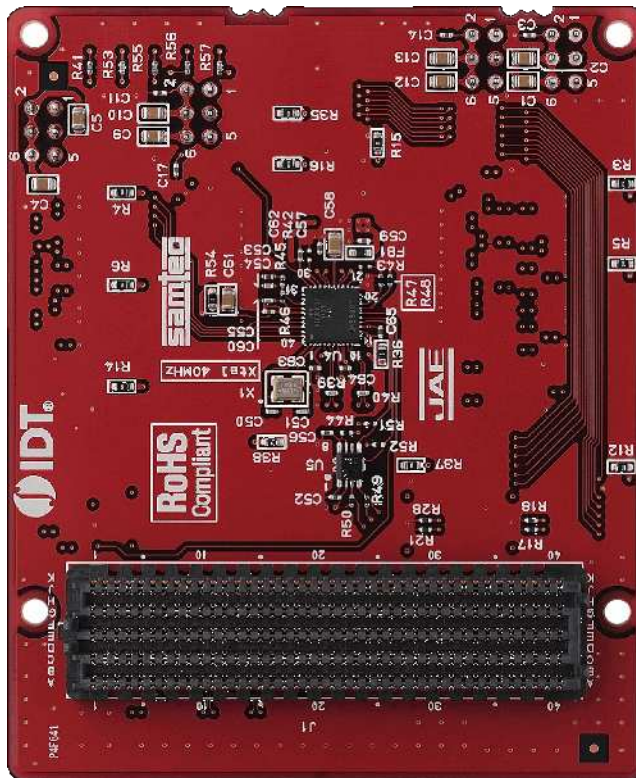


Figure 5-2 Solder Side

6. Board Specifications

The board specifications are as follows:

| | |
|----------------------|-----------------------|
| External dimensions: | W:84 mm x H:69 mm |
| Number of layers: | 10 Layers |
| Board thickness: | 1.6 mm |
| Material: | FR-4 |
| FMC connector: | Samtec' ASP-134488-01 |
| SerDes connector: | JAE' FI-RE51S-VF |
| LVDS connector: | JAE' FI-RE51S-VF |

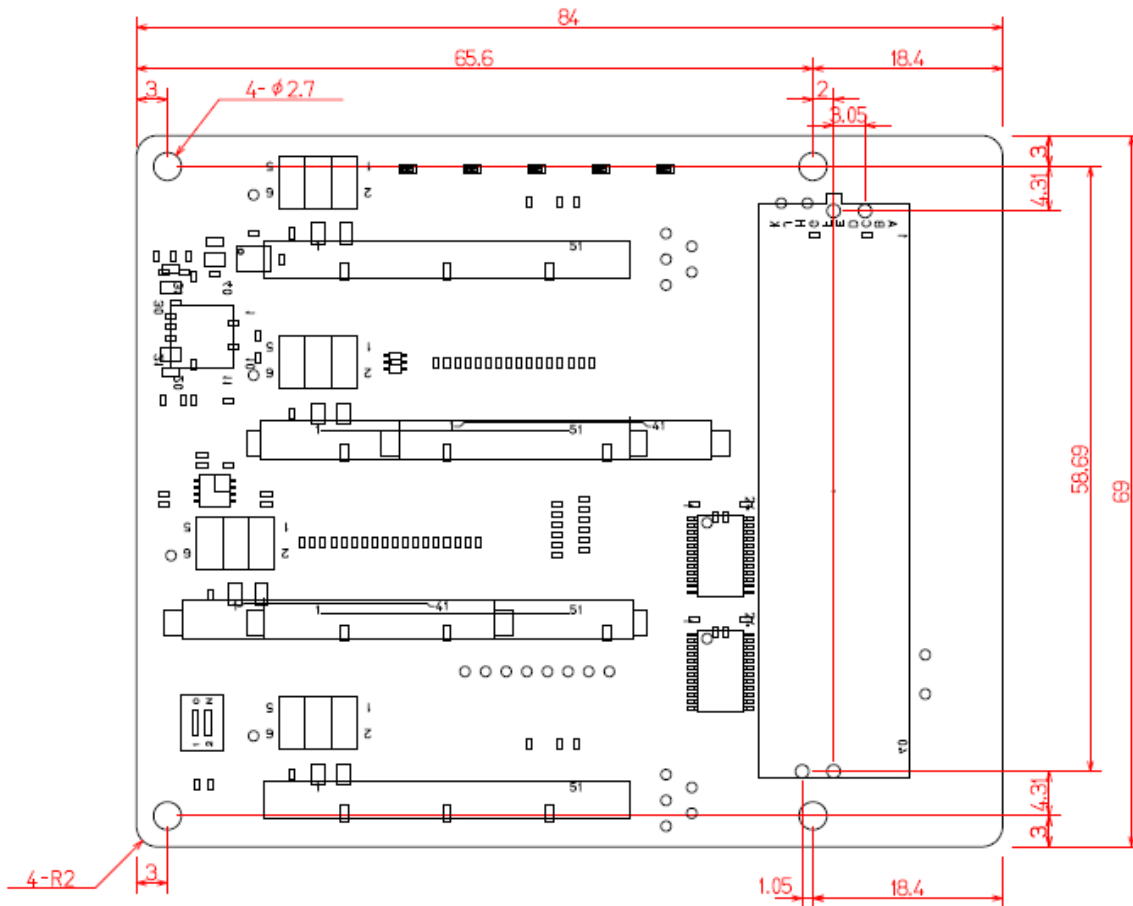


Figure 6-1 Board Dimensions

7. Description of Components

7.1. Signal connections between SerDes/LVDS and FMC connectors

Figure 7-1 shows a cable and Table 7-1 shows pin assignment of SerDes/LVDS via FMC connector. The SerDes side of the connector provides two circuits, RX1 (Receive) and TX1 (Send). The LVDS side of the connector can be used for either Receive or Send circuit.

Two dedicated cables, one for V-by-One HS and the other for LVDS, are supplied with your board. The former cable is labeled as “VBY1-51” and the latter is labeled as “LVDS”.

Be sure to use the corresponding cable for each connector.



Figure 7-1 Supplied Cables

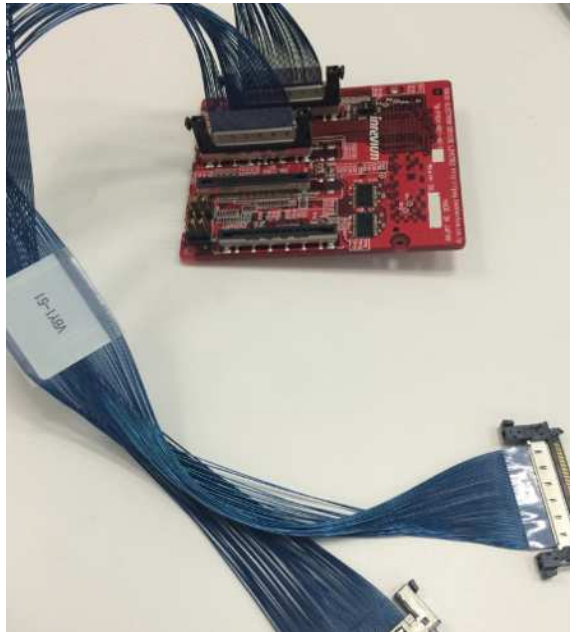


Figure 7-2 Cable Connections

Table 7-1 VBY1-RX (J2) Signal Connection

| SerDes Side Pin No. | Signal Name | FMC Side | |
|-------------------------------|-----------------|----------|--------------|
| | | Pin No. | FMC Pin Name |
| 1,2,3,4 | *1 VCC | - | - |
| 27,30,33,36,39,42,45 48,51 | GND | - | GND |
| 25 | *2 VX1_RX_HTPDN | G9 | LA03_P |
| 26 | *2 VX1_RX_LOCKN | G10 | LA03_N |
| 28 | VX1_RX0N | C7 | DP0_M2C_N |
| 29 | VX1_RX0P | C6 | DP0_M2C_P |
| 31 | VX1_RX1N | A3 | DP1_M2C_N |
| 32 | VX1_RX1P | A2 | DP1_M2C_P |
| 34 | VX1_RX2N | A7 | DP2_M2C_N |
| 35 | VX1_RX2P | A6 | DP2_M2C_P |
| 37 | VX1_RX3N | A11 | DP3_M2C_N |
| 38 | VX1_RX3P | A10 | DP3_M2C_P |
| 40 | VX1_RX4N | A15 | DP4_M2C_N |
| 41 | VX1_RX4P | A14 | DP4_M2C_P |
| 43 | VX1_RX5N | A19 | DP5_M2C_N |
| 44 | VX1_RX5P | A18 | DP5_M2C_P |
| 46 | VX1_RX6N | B17 | DP6_M2C_N |
| 47 | VX1_RX6P | B16 | DP6_M2C_P |
| 49 | VX1_RX7N | B13 | DP7_M2C_N |
| 50 | VX1_RX7P | B12 | DP7_M2C_P |

- *1: Either 12V, 3.3V or VADJ that is supplied from the FMC connector can be selected using JP4. For more information, refer to section 7.3, Power supply to the connector.
- *2: A tri-state buffer is inserted between the FMC connector and the VBY1-RX(J2) connector. For more information, refer to section 7.4, Option pin configuration of the VBY1-RX (J2) connector.

Table 7-2 VBY1-TX (J3) Signal Connection

| SerDes Side Pin No. | Signal Name | FMC Side | |
|----------------------------|--------------|----------|--------------|
| | | Pin No. | FMC Pin Name |
| 48,49,50,51 | *1 VCC | - | - |
| 1,4,7,10,13,16,19,22 25 | GND | - | GND |
| 27 | VX1_TX_HTPDN | G12 | LA08_P |
| 26 | VX1_TX_LOCKN | G13 | LA08_N |
| 24 | TX1_0_N | C3 | DP0_C2M_N |
| 23 | TX1_0_P | C2 | DP0_C2M_P |
| 21 | TX1_1_N | A23 | DP1_C2M_N |
| 20 | TX1_1_P | A22 | DP1_C2M_P |
| 18 | TX1_2_N | A27 | DP2_C2M_N |
| 17 | TX1_2_P | A26 | DP2_C2M_P |
| 15 | TX1_3_N | A31 | DP3_C2M_N |
| 14 | TX1_3_P | A30 | DP3_C2M_P |
| 12 | TX1_4_N | A35 | DP4_C2M_N |
| 11 | TX1_4_P | A34 | DP4_C2M_P |
| 9 | TX1_5_N | A39 | DP5_C2M_N |
| 8 | TX1_5_P | A38 | DP5_C2M_P |
| 6 | TX1_6_N | B37 | DP6_C2M_N |
| 5 | TX1_6_P | B36 | DP6_C2M_P |
| 3 | TX1_7_N | B33 | DP7_C2M_N |
| 2 | TX1_7_P | B32 | DP7_C2M_P |
| 39 | *2 OPT11 | G31 | LA29_N |
| 38 | *2 OPT10 | G30 | LA29_P |
| 37 | *2 OPT9 | G28 | LA25_N |
| 36 | *2 OPT8 | G27 | LA25_P |
| 35 | *2 OPT7 | G22 | LA20_N |
| 34 | *2 OPT6 | G21 | LA20_P |
| 33 | *2 OPT5 | G31 | LA29_N |
| 32 | *2 OPT4 | G30 | LA29_P |
| 31 | *2 OPT3 | G28 | LA25_N |
| 30 | *2 OPT2 | G27 | LA25_P |
| 29 | *2 OPT1 | G22 | LA20_N |
| 28 | *2 OPT0 | G21 | LA20_P |

*1: Either 12V, 3.3V or VADJ that is supplied from the FMC connector can be selected using JP3. For more information, refer to section 7.3, Power supply to the connector.

*2: The connection destination can be changed by swapping an associated resistor. For more information, refer to section 7.5, Option pin configuration of the VBY1-TX (J3) connector.

Table 7-3 LVDS-1 (CN1) Signal Connection

| LVDS Side Pin No. | Signal Name | FMC Side | |
|--------------------------------------|-------------|----------|--------------|
| | | Pin No. | FMC Pin Name |
| 1,2,3,4,5 | *VCC | - | - |
| 7,8,9,16,19,24,31,34, 39,42,48,51 | GND | - | GND |
| 10 | A_TLA0_N | H8 | LA02_N |
| 11 | A_TLA0_P | H7 | LA02_P |
| 12 | A_TLB0_N | H11 | LA04_N |
| 13 | A_TLB0_P | H10 | LA04_P |
| 14 | A_TLC0_N | H14 | LA07_N |
| 15 | A_TLC0_P | H13 | LA07_P |
| 17 | A_TLCLK0_N | H5 | CLK0_M2C_N |
| 18 | A_TLCLK0_P | H4 | CLK0_M2C_P |
| 20 | A_TLD0_N | H17 | LA11_N |
| 21 | A_TLD0_P | H16 | LA11_P |
| 22 | A_TLE0_N | H20 | LA15_N |
| 23 | A_TLE0_P | H19 | LA15_P |
| 25 | A_TLA1_N | H23 | LA19_N |
| 26 | A_TLA1_P | H22 | LA19_P |
| 27 | A_TLB1_N | H26 | LA21_N |
| 28 | A_TLB1_P | H25 | LA21_P |
| 29 | A_TLC1_N | H28 | LA24_N |
| 30 | A_TLC1_P | H29 | LA24_P |
| 32 | A_TLCLK1_N | H32 | LA28_N |
| 33 | A_TLCLK1_P | H31 | LA28_P |
| 35 | A_TLD1_N | H35 | LA30_N |
| 36 | A_TLD1_P | H34 | LA30_P |
| 37 | A_TLE1_N | H38 | LA32_N |
| 38 | A_TLE1_P | H37 | LA32_P |
| 40 | A_TLF_N0 | G34 | LA31_N |
| 41 | A_TLF_P0 | G33 | LA31_P |
| 49 | A_TLF_N1 | G37 | LA33_N |
| 50 | A_TLF_P1 | G36 | LA33_P |

*1: Either 12V, 3.3V or VADJ that is supplied from the FMC connector can be selected using JP1.
For more information, refer to section 7.3, Power supply to the connector.

Table 7-4 LVDS-2 (CN2) Signal Connection

| LVDS Side Pin No. | Signal Name | FMC Side | |
|--------------------------------------|-------------|----------|--------------|
| | | Pin No. | FMC Pin Name |
| 1,2,3,4,5 | *VCC | - | - |
| 7,8,9,16,19,24,31,34, 39,42,48,51 | GND | - | GND |
| 10 | B_TLA0_N | D9 | LA01_N_CC |
| 11 | B_TLA0_P | D8 | LA01_P_CC |
| 12 | B_TLB0_N | C11 | LA06_N |
| 13 | B_TLB0_P | C10 | LA06_P |
| 14 | B_TLC0_N | D12 | LA05_N |
| 15 | B_TLC0_P | D11 | LA05_P |
| 17 | B_TLCLK0_N | G3 | CLK1_M2C_N |
| 18 | B_TLCLK0_P | G2 | CLK1_M2C_P |
| 20 | B_TLD0_N | G7 | LA00_N_CC |
| 21 | B_TLD0_P | G6 | LA00_P_CC |
| 22 | B_TLE0_N | D15 | LA09_N |
| 23 | B_TLE0_P | D14 | LA09_P |
| 25 | B_TLA1_N | C15 | LA10_N |
| 26 | B_TLA1_P | C14 | LA10_P |
| 27 | B_TLB1_N | D18 | LA13_N |
| 28 | B_TLB1_P | D17 | LA13_P |
| 29 | B_TLC1_N | C19 | LA14_N |
| 30 | B_TLC1_P | C18 | LA14_P |
| 32 | B_TLCLK1_N | D21 | LA17_N_CC |
| 33 | B_TLCLK1_P | D20 | LA17_P_CC |
| 35 | B_TLD1_N | C23 | LA18_N_CC |
| 36 | B_TLD1_P | C22 | LA18_P_CC |
| 37 | B_TLE1_N | D24 | LA23_N |
| 38 | B_TLE1_P | D23 | LA23_P |
| 40 | B_TLF_N0 | D27 | LA26_N |
| 41 | B_TLF_P0 | D26 | LA26_P |
| 49 | B_TLF_N1 | C27 | LA27_N |
| 50 | B_TLF_P1 | C26 | LA27_P |

*1: Either 12V, 3.3V or VADJ that is supplied from the FMC connector can be selected using JP2.
For more information, refer to section 7.3, Power supply to the connector.

7.2. Customization of the SerDes connector

The board is equipped with the JAE FI-RE51S-VF. If the user wants to realize a V-by-one HS 16LANE structure, it is possible to provide a customized version of the board with the FI-RE41S-VF in accordance with the configuration of the equipment to be connected.

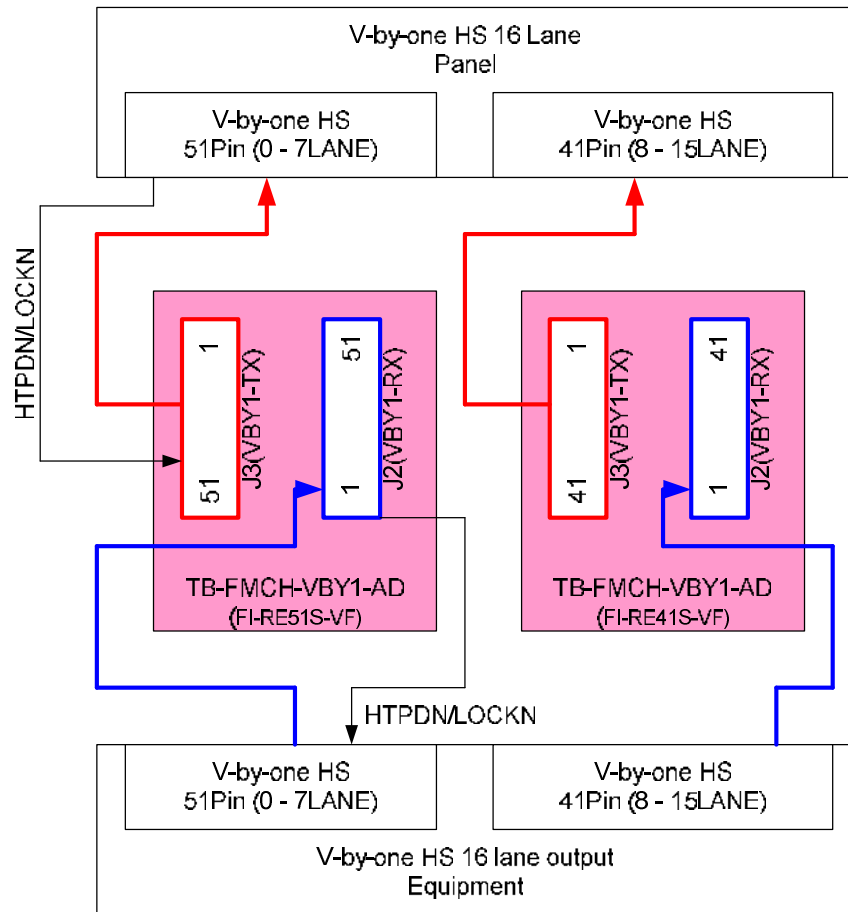


Figure 7-3 An example of the V-by-one HS 16LANE structure

If the FI-RE41S-VF is used, the HTPDN/LOCKN signal cannot be supported in V-by-oneHS protocol. Therefore, if the user wants to realize the V-by-one HS 16LANE environment, it is required to use our standard board with the FI-RE51S-VF together.

In addition, the power supply to the connector and the use of optional signals are also disabled.

For more information, please contact to us.



Figure 7-4 Overview image of the FI-RE41S-VF board

Table 7-5 VBY1-RX(J2) with FI-RE41S-VF Signal Connection

| SerDes Side | Signal Name | FMC Side | |
|-----------------------------|-------------|----------|--------------|
| Pin No. | | Pin No. | FMC Pin Name |
| 1,4,7,10,13,16,19, 22,25 | GND | - | GND |
| 2 | VX1_RX0N | C7 | DP0_M2C_N |
| 3 | VX1_RX0P | C6 | DP0_M2C_P |
| 5 | VX1_RX1N | A3 | DP1_M2C_N |
| 6 | VX1_RX1P | A2 | DP1_M2C_P |
| 8 | VX1_RX2N | A7 | DP2_M2C_N |
| 9 | VX1_RX2P | A6 | DP2_M2C_P |
| 11 | VX1_RX3N | A11 | DP3_M2C_N |
| 12 | VX1_RX3P | A10 | DP3_M2C_P |
| 14 | VX1_RX4N | A15 | DP4_M2C_N |
| 15 | VX1_RX4P | A14 | DP4_M2C_P |
| 17 | VX1_RX5N | A19 | DP5_M2C_N |
| 18 | VX1_RX5P | A18 | DP5_M2C_P |
| 20 | VX1_RX6N | B17 | DP6_M2C_N |
| 21 | VX1_RX6P | B16 | DP6_M2C_P |
| 23 | VX1_RX7N | B13 | DP7_M2C_N |
| 24 | VX1_RX7P | B12 | DP7_M2C_P |

Table 7-6 VBY1-TX(J3) with FI-RE41S-VF Signal Connection

| SerDes Side | Signal Name | FMC Side | |
|--------------------------------|-------------|----------|--------------|
| Pin No. | | Pin No. | FMC Pin Name |
| 17,20,23,26,29,32,35, 38,41 | GND | - | GND |
| 40 | TX1_0_N | C3 | DP0_C2M_N |
| 39 | TX1_0_P | C2 | DP0_C2M_P |
| 37 | TX1_1_N | A23 | DP1_C2M_N |
| 36 | TX1_1_P | A22 | DP1_C2M_P |
| 34 | TX1_2_N | A27 | DP2_C2M_N |
| 33 | TX1_2_P | A26 | DP2_C2M_P |
| 31 | TX1_3_N | A31 | DP3_C2M_N |
| 30 | TX1_3_P | A30 | DP3_C2M_P |
| 28 | TX1_4_N | A35 | DP4_C2M_N |
| 27 | TX1_4_P | A34 | DP4_C2M_P |
| 25 | TX1_5_N | A39 | DP5_C2M_N |
| 24 | TX1_5_P | A38 | DP5_C2M_P |
| 22 | TX1_6_N | B37 | DP6_C2M_N |
| 21 | TX1_6_P | B36 | DP6_C2M_P |
| 19 | TX1_7_N | B33 | DP7_C2M_N |
| 18 | TX1_7_P | B32 | DP7_C2M_P |

7.3. Power supply to the connector

Power supply from the FMC connector to each connector can be switched using the onboard jumper pins. Figure 7-5 shows the structure of power supply.

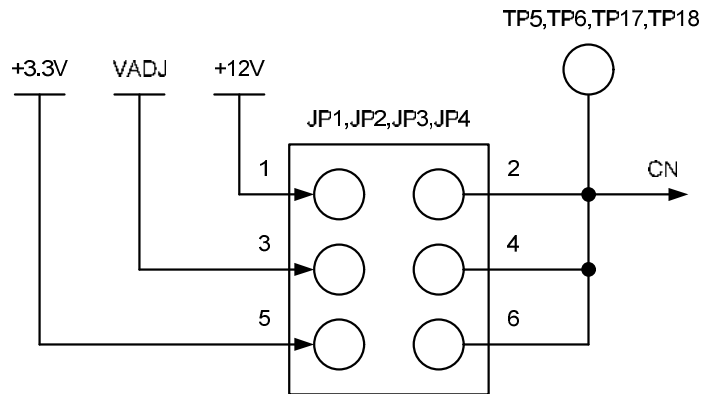


Figure 7-5 SerDes/LVDS CN Power Supply

Table 7-7 Power Supply Switching

| CN Name | Pin No. | Connect(JP1.2.3.4) | | | |
|-------------|-------------|--------------------|------|------|------------|
| | | 1-2 | 3-4 | 5-6 | Test Point |
| CN1(LVDS-1) | 1,2,3,4,5 | 12V | VADJ | 3.3V | TP5 |
| CN2(LVDS-2) | 1,2,3,4,5 | 12V | VADJ | 3.3V | TP6 |
| J2(VB1-TX) | 48,49,50,51 | 12V | VADJ | 3.3V | TP17 |
| J3(VB1-RX) | 1,2,3,4,5 | 12V | VADJ | 3.3V | TP18 |

7.4. Option pin configuration of the VBY1-RX (J2) connector

A tri-state buffer is inserted in the signal connection between the VBY1-RX(J2) connector and the FMC connector for the VX1_RX_HTPDN and VX1_RX_LOCKN pins.

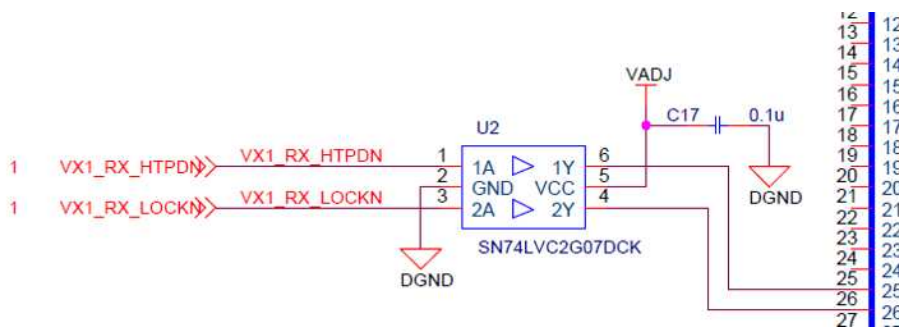


Figure 7-6 A Tri-State Buffer Structure

Normally the tri-state output is performed from the FPGA in V-by-One HS protocol. However, if the board is used, perform the drive output.

7.5. Option pin configuration of the VBY1-TX (J3) connector

In the connection structure shown in Figure 7-7, 12 option pins are provided for signal connections between the FMC connector and the VBY1-TX (J3) connector via the level conversion IC (VADJ => 3.3V conversion). 6 signals are connected via zero ohm resistors in default setting.

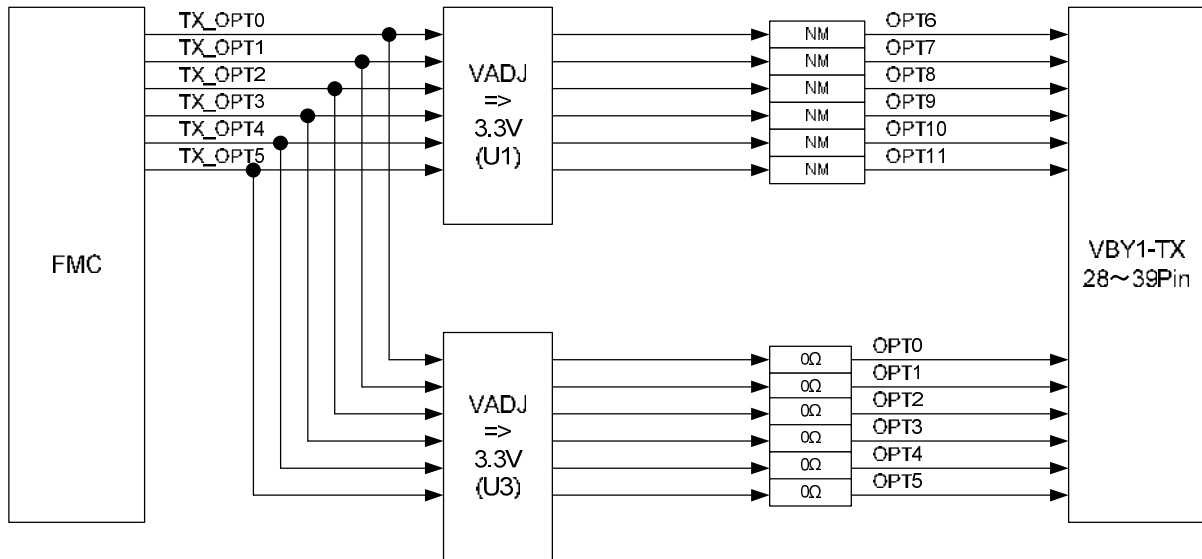


Figure 7-7 VBY1-TX(J3) Option Pin Connections

7.6. Option pin configuration of connectors

The VBY1-TX (J3)/LVDS-1(CN1)/LVDS-2(CN2) connectors have several test points.

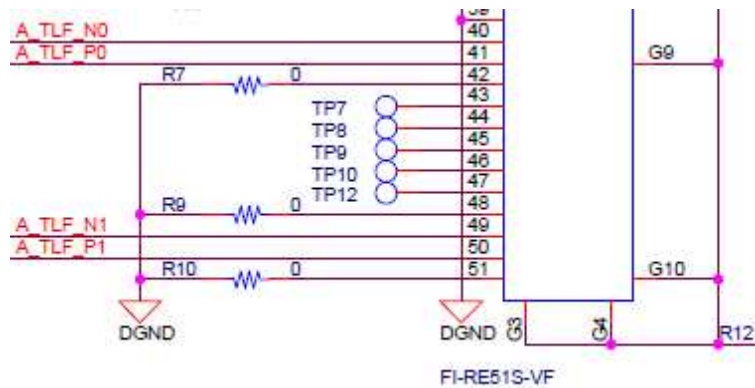


Figure 7-8 LVDS-1(CN1) Test Points

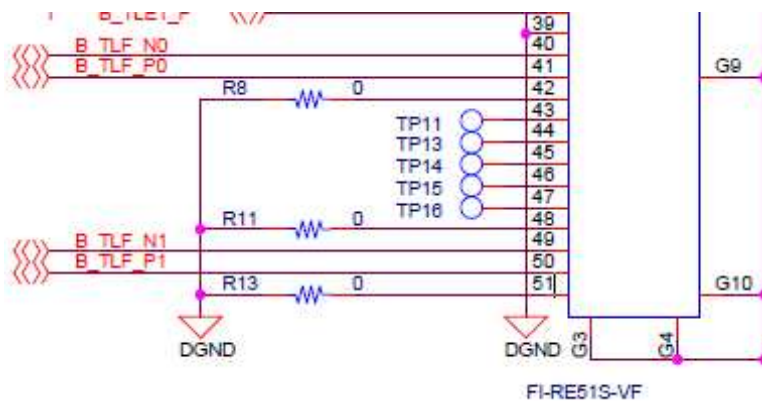


Figure 7-9 LVDS-1(CN2) Test Points

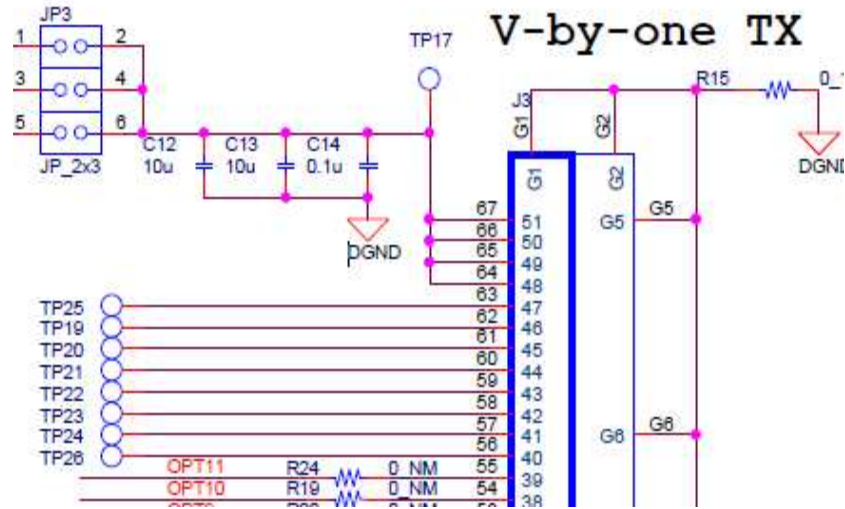


Figure 7-10 VBY1-TX(J3) Test Points

7.7. Reference Clock

The Board is equipped with IDT's PLL ICS849N202I and can provide a reference clock to the transceiver of the FPGA to be connected.

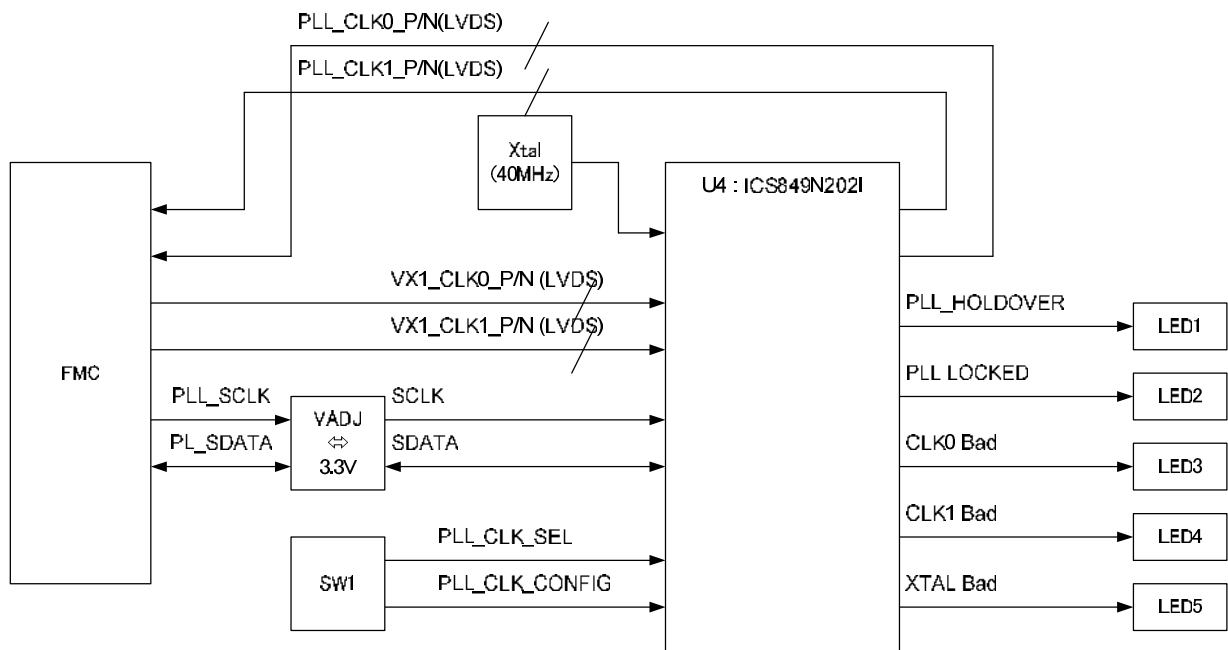


Figure 7-11 PLL Connection Diagram

7.7.1. Output frequency setting

The onboard switch (SW1-1) allows selection of the desired output frequency by turning it to the ON or OFF position.

OFF => 148.5MHz output ON => 74.25MHz output

This PLL has 2 different clock sources but it generates the same frequency irrespective of the setting.

If it receives a supplied clock (74.25MHz LVDS) from the connected device, it generates a clock in synchronization with it. It allows selection of 2 different clock sources by setting the onboard switch (SW1-2).

OFF => VX1_CLK0_P/N ON => VX1_CLK1_P/N

7.7.2. Changing I2C setting

This PLL allows I2C access to the PLL registers from the FPGA via the level convertor.

We have performed an operation check of the ## I2C but do not provide the FPGA design.

For more information, please contact us.

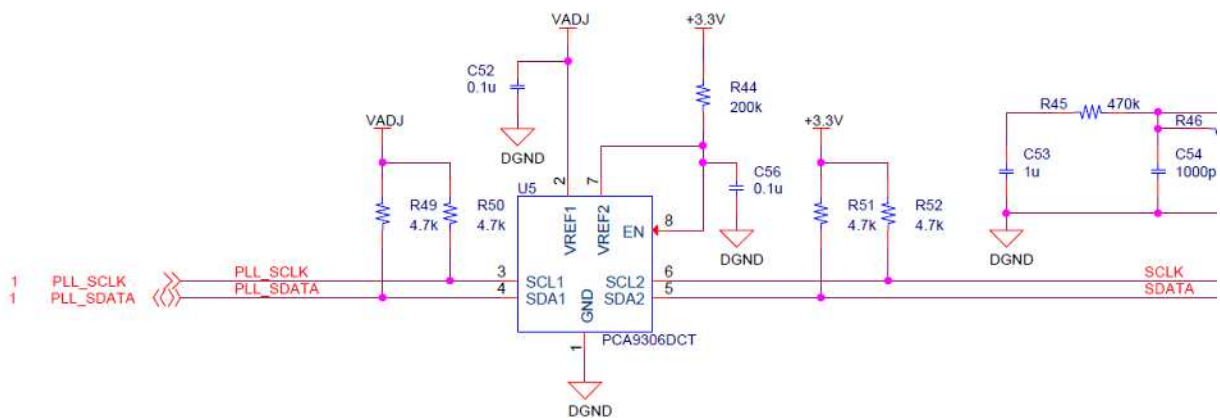


Figure 7-12 PLL I2C Connection Diagram

7.7.3. FMC to PLL Connection

Following Table provides the information relating to the FMC to PLL connection.

Table 7-8: FMC to PLL Signal Connection

| PLL Side | | FMC Side | |
|----------|-------------|----------|---------------|
| Pin No. | Signal Name | Pin No. | FMC Pin Name |
| 5 | VX1_CLK0_P | G15 | LA12_P |
| 6 | VX1_CLK0_N | G16 | LA12_N |
| 9 | VX1_CLK1_P | G18 | LA016_P |
| 10 | VX1_CLK1_N | G19 | LA016_N |
| 14 | PLL_SDATA | G25 | LA22_N |
| 15 | PLL_SCLK | G24 | LA22_P |
| 27 | PLL_CLK0_P | D4 | GBTCLK0_M2C_P |
| 26 | PLL_CLK0_N | D5 | GBTCLK0_M2C_N |
| 24 | PLL_CLK1_P | B20 | GBTCLK1_M2C_P |
| 23 | PLL_CLK1_N | B21 | GBTCLK1_M2C_N |

7.7.4. PLL STATUS Output

Following Table provides the information relating to those LEDs that are connected to the STATUS signal from the PLL.

Table 7-9 PLL LED STATUS

| LED No. | PLL Pin Name | STATUS |
|---------|--------------|--|
| LED1 | HOLDOVER | Lights when the PLL gets unlocked. |
| LED2 | CONFIG | Lights when the PLL gets locked. |
| LED3 | CLK0BAD | Lights when the VX1_CLK0_P/N is not input. |
| LED4 | CLK1BAD | Lights when the VX1_CLK1_P/N is not input. |
| LED5 | XTALBAD | Lights when the Xtal(40MHz) is failed. |

8. Default Switch Settings

Following Table shows the default switch settings.

Table8-1 Default Settings

| No. | Silk No. | Initial Setting | Function |
|-----|----------|-----------------|--|
| 1 | JP1 | Open | Power supply selection (12V/3.3V/VADJ) |
| 2 | JP2 | Open | Power supply selection (12V/3.3V/VADJ) |
| 3 | JP3 | Open | Power supply selection (12V/3.3V/VADJ) |
| 4 | JP4 | Open | Power supply selection (12V/3.3V/VADJ) |
| 5 | SW1-1 | OFF | PLL output frequency selection |
| 6 | SW1-2 | OFF | PLL input clock selection |

The short-circuit socket comes with the Board.



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